

LAN8740/LAN8740i

Small Footprint MII/RMII 10/100 Energy Efficient Ethernet Transceiver with HP Auto-MDIX and flexPWR[®] Technology



PRODUCT FEATURES

Data Brief

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Compliant with Energy Efficient Ethernet 802.3az
- Cable diagnostic support
- Wake on LAN (WoL) support
- Comprehensive flexPWR[®] technology
 - Flexible power management architecture
 - LVCMOS Variable I/O voltage range: +1.8 V to +3.3 V
 - Integrated 1.2 V regulator with disable feature
- HP Auto-MDIX support
- Small footprint 32-pin SQFN lead-free RoHS compliant package (5 x 5 x 0.9 mm height)

Target Applications

- Set-Top Boxes
- Networked Printers and Servers
- Test Instrumentation
- LAN on Motherboard
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adaptors/Servers
- Gaming Consoles
- POE Applications (Refer to SMSC Application Note 17.18)

Key Benefits

- High-performance 10/100 Ethernet transceiver
 - Compliant with IEEE802.3/802.3u (Fast Ethernet)
 - Compliant with ISO 802-3/IEEE 802.3 (10BASE-T)
 - Compliant with Energy Efficient Ethernet IEEE 802.3az
 - Loop-back modes
 - Auto-negotiation
 - Automatic polarity detection and correction
 - Link status change wake-up detection
 - Vendor specific register functions
 - Supports both MII and the reduced pin count RMII interfaces

Power and I/Os

- Various low power modes
- Integrated power-on reset circuit
- Two status LED outputs
- May be used with a single 3.3 V supply

Additional Features

Ability to use a low cost 25 MHz crystal for reduced BOM

Packaging

 32-pin SQFN (5 x 5 mm) lead-free RoHS compliant package with MII and RMII

Environmental

- Commercial temperature range (0°C to +70°C)
- Industrial temperature range (-40°C to +85°C)



ORDER NUMBER(S):

LAN8740-EN (Tray) for 32-pin, SQFN lead-free RoHS compliant package (0°C to +70°C temp)

LAN8740i-EN (Tray) for 32-pin, SQFN lead-free RoHS compliant package (-40°C to +85°C temp)

LAN8740-EN-TR (Tape & Reel) for 32-pin, SQFN lead-free RoHS compliant package (0°C to +70°C temp)

LAN8740i-EN-TR (Tape & Reel) for 32-pin, SQFN lead-free RoHS compliant package (-40 to +85°C temp)

This product meets the halogen maximum concentration values per IEC61249-2-21 For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.



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General Description

The LAN8740/LAN8740i is a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3, 802.3u, and 802.3az (Energy Efficient Ethernet) standards. Energy Efficient Ethernet (EEE) support results in significant power savings during low link utilizations.

The LAN8740/LAN8740i supports communication with an Ethernet MAC via a standard MII (IEEE 802.3u)/RMII interface. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10 Mbps (10BASE-T) and 100 Mbps (100BASE-TX) operation. The LAN8740/LAN8740i implements autonegotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables. Integrated Wake on LAN (WoL) support provides a mechanism to trigger an interrupt upon reception of a perfect DA, broadcast, magic packet, or wakeup frame.

The LAN8740/LAN8740i supports both IEEE 802.3-2005 compliant and vendor-specific register functions. However, no register access is required for operation. The initial configuration may be selected via the configuration pins. Register-selectable configuration options may be used to further define the functionality of the transceiver.

The LAN8740/LAN8740i can be programmed to support wake-on-LAN at the physical layer, allowing detection of configurable Wake-up Frame and Magic packets. This feature allows filtering of packets at the PHY layer, without requiring MAC intervention. Additionally, the LAN8740/LAN8740i supports cable diagnostics which allow the device to identify opens/shorts and their location on the cable via vendor-specific registers.

Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6 V. The device can be configured to operate on a single 3.3 V supply utilizing an integrated 3.3 V to 1.2 V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN8740/LAN8740i is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range versions. A typical system application is shown in Figure 1. Figure 2 provides an internal block diagram of the device.

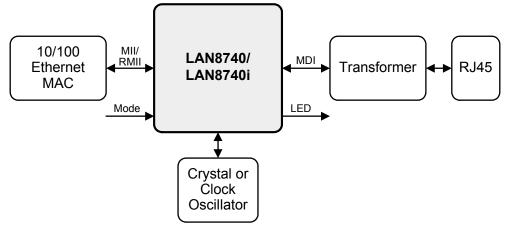


Figure 1 System Block Diagram



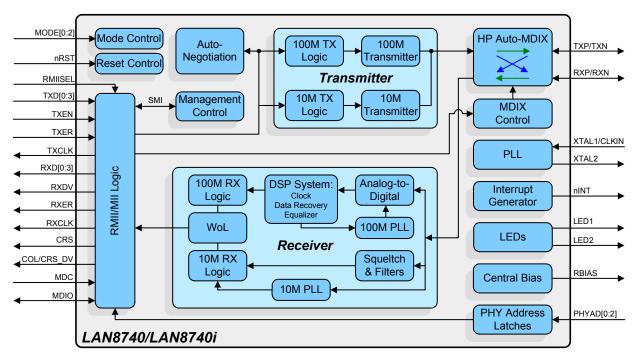
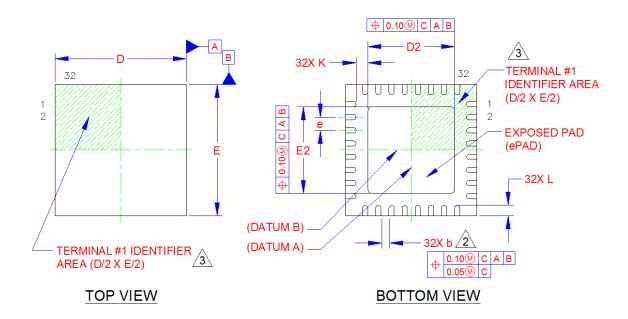


Figure 2 Architectural Overview



Package Outline



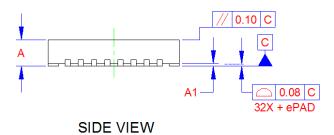


Figure 3 32-SQFN Package

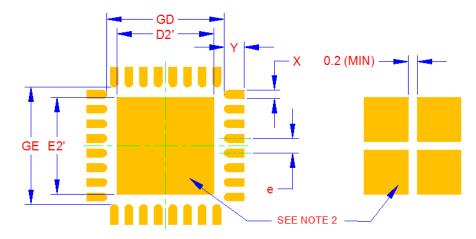
NOMINAL REMARKS MIN MAX 0.80 0.90 1.00 Overall Package Height Α A1 0 0.02 0.05 Standoff D/E 4.90 5.00 5.10 X/Y Body Size D2/E2 3.20 3.30 3.40 X/Y Exposed Pad Size 0.40 0.45 Terminal Length 0.35 Terminal Width 0.18 0.25 b 0.30 0.35 Pin to Exposed Pad Clearance 0.45 k 0.50 BSC Terminal Pitch е

Table 1 32-SQFN Dimensions

Notes:

- 1. All dimensions are in millimeters unless otherwise noted.
- 2. Dimension "b" applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
- 3. The pin 1 identifier may vary, but is always located within the zone indicated.





LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	4.00	-	4.10
D2'/E2'	-	3.30	3.30
X	-	0.28	0.28
Y	-	0.69	-
е		0.50	

NOTES:

- THE USER MAY MODIFY THE PCB LAND PATTERN DESIGN AND DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY
- 2. EXPOSED SOLDERABLE COPPER AREA OF THE CENTER PAD CAN BE EITHER SOLID OR SEGMENTED
- 3. MAXIMUM THERMAL AND ELECTRICAL PACKAGE PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN

Figure 4 Recommended PCB Land Pattern

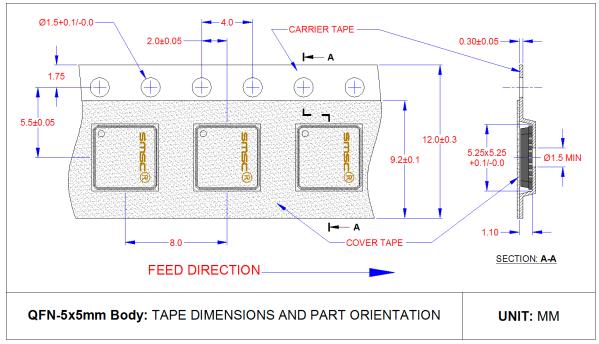


Figure 5 Taping Dimensions and Part Orientation



2.0 (±0.5)

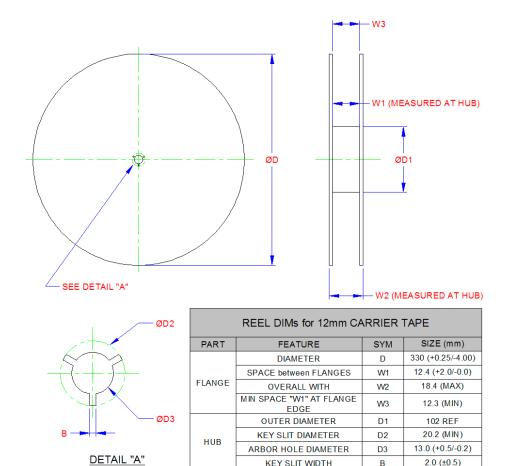


Figure 6 Reel Dimensions

KEY SLIT WIDTH

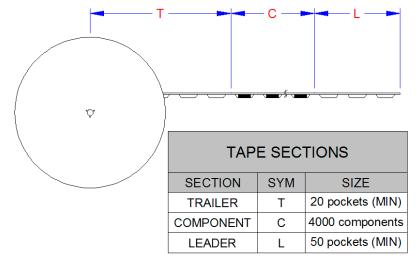


Figure 7 Tape Length and Part Quantity

Note: Standard reel size is 4,000 pieces per reel.