## FEATURES

## Computes:

True rms value
Average rectified value
Absolute value

## Provides:

200 mV full-scale input range (larger inputs with input attenuator)
Direct interfacing with 3 1/2 digit CMOS ADCs
High input impedance: $10^{12} \Omega$
Low input bias current: 25 pA max
High accuracy: $\pm 0.2 \mathrm{mV} \pm 0.3 \%$ of reading
RMS conversion with signal crest factors up to 5
Wide power supply range: $\pm \mathbf{2 . 5} \mathrm{V}$ to $\pm \mathbf{1 6 . 5} \mathrm{V}$
Low power: $160 \mu \mathrm{~A}$ max supply current
No external trims needed for specified accuracy
AD736-a general-purpose, buffered voltage output version also available

## GENERAL DESCRIPTION

The AD737 ${ }^{1}$ is a low power, precision, monolithic true rms-todc converter. It is laser trimmed to provide a maximum error of $\pm 0.2 \mathrm{mV} \pm 0.3 \%$ of reading with sine wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty-cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms precision rectifiers in many applications. Compared to these circuits, the AD737 offers higher accuracy at equal or lower cost.

The AD737 can compute the rms value of both ac and dc input voltages. It can also be operated ac-coupled by adding one external capacitor. In this mode, the AD737 can resolve input signal levels of $100 \mu \mathrm{~V}$ rms or less, despite variations in temperature or supply voltage. High accuracy is also maintained for input waveforms with crest factors of 1 to 3 . In addition, crest factors as high as 5 can be measured (while introducing only $2.5 \%$ additional error) at the 200 mV full-scale input level.

The AD737 has no output buffer amplifier, thereby significantly reducing dc offset errors occurring at the output, which makes the device highly compatible with high input impedance ADCs.

[^0]Rev. F
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.


Figure 1.
Requiring only $160 \mu \mathrm{~A}$ of power supply current, the AD737 is optimized for use in portable multimeters and other batterypowered applications. This converter also provides a powerdown feature that reduces the power-supply standby current to less than $30 \mu \mathrm{~A}$.

Two signal input terminals are provided in the AD737. A high impedance ( $10^{12} \Omega$ ) FET input interfaces directly with high R input attenuators, and a low impedance ( $8 \mathrm{k} \Omega$ ) input accepts rms voltages to 0.9 V while operating from the minimum power supply voltage of $\pm 2.5 \mathrm{~V}$. The two inputs can be used either single-ended or differentially.

The AD737 achieves $1 \%$ of reading error bandwidth, exceeding 10 kHz for input amplitudes from 20 mV rms to 200 mV rms while consuming only 0.72 mW .

The AD737 is available in four performance grades. The AD737J and AD737K grades are rated over the commercial temperature range of $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$. The AD737JR- 5 is tested with supply voltages of $\pm 2.5 \mathrm{~V} \mathrm{dc}$. The AD737A and AD737B grades are rated over the industrial temperature range of $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. The AD737 is available in three low cost, 8 -lead packages: PDIP, SOIC, and CERDIP.

## PRODUCT HIGHLIGHTS

1. The AD737 is capable of computing the average rectified value, absolute value, or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD737 to perform true rms measurement.
3. The low power consumption of 0.72 mW makes the AD737 suitable for battery-powered applications.
[^1]
## AD737

## TABLE OF CONTENTS

Specifications ..... 3
Absolute Maximum Ratings .....  5
ESD Caution ..... 5
Pin Configurations and Function Descriptions ..... 6
Typical Performance Characteristics ..... 7
Calculating Settling Time ..... 10
Types of AC Measurement ..... 10
Theory of Operation ..... 12
RMS Measurement-Choosing Optimum Value For Cav ..... 12
REVISION HISTORY
1/05—Rev. E to Rev. F
Updated Format Universal
Added Functional Block Diagram ..... 1
Changes to General Description Section ..... 1
Changes to Pin Configurations and Function Descriptions Section .....  6
Changes to Typical Performance Characteristics Section ..... 7
Changes to Table 4 ..... 11
Change to Figure 24 ..... 12
Change to Figure 27 ..... 15
Changes to Ordering Guide ..... 18
6/03-Rev. D to Rev. E
Added AD737JR-5 ..... Universal
Changes to FEATURES .....  1
Changes to GENERAL DESCRIPTION ..... 1
Changes to SPECIFICATIONS ..... 2
Changes to ABSOLUTE MAXIMUM RATINGS ..... 4
Changes to ORDERING GUIDE .....  4
Added TPCs 16 through 19 .....  6
Changes to Figures 1 and 2 ..... 8
Changes to Figure 8 ..... 11
Updated OUTLINE DIMENSIONS ..... 12
Rapid Settling Times via the Average Responding Connection ..... 12
DC Error, Output Ripple, and Averaging Error ..... 13
Ac Measurement Accuracy and Crest Factor ..... 13
Selecting Practical Values for Capacitors ..... 13
Application Circuits ..... 15
Outline Dimensions ..... 17
Ordering Guide ..... 18
12/02-Rev. C to Rev. D
Changes to FUNCTIONAL BLOCK DIAGRAM ..... 1
Changes to PIN CONFIGURATION .....  4
Figure 1 replaced .....  8
Changes to Figure 2. .....  8
Figure 5 replaced ..... 10
Changes to Application Circuits Figures 4, 6-8 ..... 10
OUTLINE DIMENSIONS updated ..... 12
12/99—Rev. B to Rev. C

## SPECIFICATIONS

$\mathrm{T}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V}$ supplies, except AD737J-5, $\pm 2.5 \mathrm{~V}, \mathrm{C}_{\mathrm{AV}}=33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{C}}=10 \mu \mathrm{~F}, \mathrm{f}=1 \mathrm{kHz}$, sine wave input applied to Pin 2 , unless otherwise specified. Specifications shown in boldface are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.
Table 1.


## AD737


${ }^{1}$ POR $=\%$ of reading.
${ }^{2}$ Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 V and 200 mV rms .
${ }^{3}$ After fourth-order error correction using the equation $y=-0.31009 x^{4}-0.21692 x^{3}-0.06939 x^{2}+0.99756 x+11.1 \times 10^{-6}$, where $y$ is the corrected result and $x$ is the device output between 0.01 V and 0.3 V .
${ }^{4}$ Crest factor error is specified as the additional error resulting from the specific crest factor, using a 200 mV rms signal as a reference. The crest factor is defined as $V_{\text {Peak } / V ~ r m s . ~}^{\text {r }}$
${ }^{5}$ DC offset does not limit ac resolution.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
| :--- | :--- |
| Supply Voltage | $\pm 16.5 \mathrm{~V}$ |
| Internal Power Dissipation ${ }^{1}$ | 200 mW |
| Input Voltage | $\pm \mathrm{V}_{\mathrm{s}}$ |
| Output Short-Circuit Duration | Indefinite |
| Differential Input Voltage | $+\mathrm{V}_{\mathrm{s}}$ and $-\mathrm{V}_{\mathrm{s}}$ |
| Storage Temperature Range (Q) | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Storage Temperature Range (N, R) | $-65^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Lead Temperature Range (Soldering 60 sec$)$ | $300^{\circ} \mathrm{C}$ |
| ESD Rating | 500 V |

[^2]
## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Figure 2. R-8 (SOIC) Pin Configuration


Figure 3. Q-8 (CERDIP) Pin Configuration


Figure 4. N-8 (PDIP) Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
| :--- | :--- | :--- |
| 1 | $\mathrm{C}_{\mathrm{C}}$ | Coupling Capacitor for Indirect DC Coupling. |
| 2 | VIN | RMS Input. |
| 3 | POWER DOWN | Disables the AD737. Low is enabled; high is powered-down. |
| 4 | $-\mathrm{V}_{S}$ | Negative Power Supply. |
| 5 | CAV | Averaging Capacitor. |
| 6 | OUTPUT | Output. |
| 7 | $+\mathrm{V}_{\mathrm{S}}$ | Positive Power Supply. |
| 8 | COM | Common. |

## TYPICAL PERFORMANCE CHARACTERISTICS

$\mathrm{T}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V}$ supplies, except AD737J-5, $\pm 2.5 \mathrm{~V}, \mathrm{C}_{\mathrm{AV}}=33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{C}}=10 \mu \mathrm{~F}, \mathrm{f}=1 \mathrm{kHz}$, sine wave input applied to Pin 2, unless otherwise specified.


Figure 5. Additional Error vs. Supply Voltage


Figure 6. Maximum Input Level vs. Supply Voltage


Figure 7. Power-Down Current vs. Supply Voltage


Figure 8. Frequency Response Driving Pin 1


Figure 9. Frequency Response Driving Pin 2


Figure 10. Additional Error vs. Crest Factor vs. Cav


Figure 11. Additional Error vs. Temperature


Figure 12. DC Supply Current vs. RMS Input Level


Figure 13. RMS Input Level vs. $-3 d B$ Frequency


Figure 14. Error vs. RMS Input Voltage Using Circuit of Figure 29


Figure 15. $C_{A V}$ vs. Frequency for Specified Averaging Error


Figure 16. RMS Input Level vs. Frequency for Specified Averaging Error


Figure 17. Input Bias Current vs. Supply Voltage


Figure 18. Settling Time vs. RMS Input Level for Various Values of $C_{A V}$


Figure 19. Input Bias Current vs. Temperature


Figure 20. Frequency Response Driving Pin 1


Figure 21. Error Contours Driving Pin 1


Figure 22. Additional Crest Factor Error for Various Values of $C_{A V}$


Figure 23. Error vs. Input Voltage Driving Pin 1

## CALCULATING SETTLING TIME

Figure 18 can be used to closely approximate the time required for the AD737 to settle when its input level is reduced in amplitude. The net time required for the rms converter to settle is the difference between two times extracted from the graph: the initial time minus the final settling time. As an example, consider the following conditions: a $33 \mu \mathrm{~F}$ averaging capacitor, an initial rms input level of 100 mV , and a final (reduced) input level of 1 mV . From Figure 18, the initial settling time (where the 100 mV line intersects the $33 \mu \mathrm{~F}$ line) is approximately 80 ms . The settling time corresponding to the new or final input level of 1 mV is approximately 8 seconds. Therefore, the net time for the circuit to settle to its new value is 8 seconds minus 80 ms , which is 7.92 seconds.

Note that because of the smooth decay characteristic inherent with a capacitor/diode combination, this is the total settling time to the final value ( $n o t$ the settling time to $1 \%, 0.1 \%$, and so on, of the final value). Also, this graph provides the worst-case settling time, because the AD737 settles very quickly with increasing input levels.

## TYPES OF AC MEASUREMENT

The AD737 is capable of measuring ac signals by operating as either an average responding or a true rms-to-dc converter. As its name implies, an average responding converter computes the average absolute value of an ac (or ac and dc) voltage or current by full wave rectifying and low-pass filtering the input signal; this approximates the average. The resulting output, a dc average level, is then scaled by adding (or reducing) gain; this scale factor converts the dc average reading to an rms equivalent value for the waveform being measured. For example, the average absolute value of a sine wave voltage is 0.636 that of $\mathrm{V}_{\text {peak }}$; the corresponding rms value is 0.707 times $\mathrm{V}_{\text {peak. }}$ Therefore, for sine wave voltages, the required scale factor is 1.11 ( 0.707 divided by 0.636 ).

In contrast to measuring the average value, true rms measurement is a universal language among waveforms, allowing the magnitudes of all types of voltage (or current) waveforms to be compared to one another and to dc. RMS is a direct measure of the power or heating value of an ac voltage compared to that of a dc voltage; an ac signal of 1 V rms produces the same amount of heat in a resistor as a 1 V dc signal.

Mathematically, the rms value of a voltage is defined (using a simplified equation) as

$$
V \mathrm{rms}=\sqrt{A v g\left(V^{2}\right)}
$$

This involves squaring the signal, taking the average, and then obtaining the square root. True rms converters are smart rectifiers; they provide an accurate rms reading regardless of the type of waveform being measured. However, average responding converters can exhibit very high errors when their input signals deviate from their precalibrated waveform; the magnitude of the error depends on the type of waveform being measured. As an example, if an average responding converter is calibrated to measure the rms value of sine wave voltages and then is used to measure either symmetrical square waves or dc voltages, the converter has a computational error $11 \%$ (of reading) higher than the true rms value (see Table 4).

Table 4. Error Introduced by an Average Responding Circuit When Measuring Common Waveforms

| Type of Waveform <br> 1 V Peak Amplitude | Crest Factor <br> (VPEAK/V rms) | True RMS <br> Value (V) | Reading of an Average Responding Circuit <br> Calibrated to an RMS Sine Wave Value (V) | Error (\%) |
| :--- | :--- | :--- | :--- | :--- |
| Undistorted Sine Wave | 1.414 | 0.707 | 0.707 | 0 |
| Symmetrical Square Wave | 1.00 | 1.00 | 1.11 | 11.0 |
| Undistorted Triangle Wave | 1.73 | 0.577 | 0.555 | -3.8 |
| Gaussian Noise |  |  |  |  |
| (98\% of Peaks <1 V) | 3 | 0.333 | 0.295 | -11.4 |
| Rectangular | 2 | 0.5 | 0.278 | -44 |
| Pulse Train | 10 | 0.1 |  | -89 |
| SCR Waveforms |  | 0.495 | 0.354 | -28 |
| 50\% Duty Cycle | 2 | 0.212 | -30 |  |

## AD737

## THEORY OF OPERATION

As shown in Figure 24, the AD737 has four functional subsections: input amplifier, full-wave rectifier, rms core, and bias section. The FET input amplifier allows both a high impedance, buffered input (Pin 2) or a low impedance, wide dynamic range input (Pin 1). The high impedance input, with its low input bias current, is well suited for use with high impedance input attenuators. The input signal can be either dc-coupled or ac-coupled to the input amplifier. Unlike other rms converters, the AD737 permits both direct and indirect ac coupling of the inputs. AC coupling is provided by placing a series capacitor between the input signal and Pin 2 (or Pin 1) for direct coupling and between Pin 1 and ground (while driving Pin 2) for indirect coupling.


Figure 24. AD737 True RMS Circuit (Test Circuit)
The output of the input amplifier drives a full-wave precision rectifier, which, in turn, drives the rms core. It is in the core that the essential rms operations of squaring, averaging, and square rooting are performed, using an external averaging capacitor, $C_{A V}$. Without $C_{A V}$, the rectified input signal travels through the core unprocessed, as is done with the average responding connection (Figure 25).

In the average responding connection, all the averaging is carried out by an RC post filter consisting of an $8 \mathrm{k} \Omega$ internal scale-factor resistor connected between Pin 6 and Pin 8, and an external averaging capacitor, $\mathrm{C}_{\mathrm{F}}$. In the rms circuit, this additional filtering stage helps reduce any output ripple that was not removed by the averaging capacitor, $\mathrm{C}_{\mathrm{Av}}$.

A final subsection, the bias section, permits a power-down function. This reduces the idle current of the AD737 from $160 \mu \mathrm{~A}$ down to a mere $30 \mu \mathrm{~A}$. This feature is selected by tying Pin 3 to the $+\mathrm{V}_{\text {s }}$ terminal.

## RMS MEASUREMENT-CHOOSING OPTIMUM VALUE FOR $\mathrm{C}_{\mathrm{Av}}$

Because the external averaging capacitor, $\mathrm{C}_{\mathrm{AV}}$, holds the rectified input signal during rms computation, its value directly affects the accuracy of the rms measurement, especially at low frequencies. Furthermore, because the averaging capacitor appears across a diode in the rms core, the averaging time constant increases exponentially as the input signal is reduced. This means that as the input level decreases, errors due to nonideal averaging decrease while the time it takes for the circuit to settle to the new rms level increases. Therefore, lower input levels allow the circuit to perform better (due to increased averaging) but increase the waiting time between measurements. When selecting $\mathrm{C}_{\mathrm{AV}}$, a trade-off between computational accuracy and settling time is required.

## RAPID SETTLING TIMES VIA THE AVERAGE RESPONDING CONNECTION

Because the average responding connection shown in Figure 25 does not use an averaging capacitor, its settling time does not vary with input signal level; it is determined solely by the RC time constant of $C_{F}$ and the internal $8 \mathrm{k} \Omega$ output scaling resistor.


Figure 25. AD737 Average Responding Circuit

## DC ERROR, OUTPUT RIPPLE, AND AVERAGING ERROR

Figure 26 shows the typical output waveform of the AD737 with a sine wave input voltage applied. As with all real-world devices, the ideal output of $\mathrm{V}_{\text {out }}=\mathrm{V}_{\text {IN }}$ is never exactly achieved; instead, the output contains both a dc and an ac error component.


Figure 26. Output Waveform for Sine Wave Input Voltage
As shown, the dc error is the difference between the average of the output signal (when all the ripple in the output has been removed by external filtering) and the ideal dc output. The dc error component is, therefore, set solely by the value of the averaging capacitor used-no amount of post filtering (using a very large $\mathrm{C}_{\mathrm{F}}$ ) allows the output voltage to equal its ideal value. The ac error component, an output ripple, can be easily removed using a large enough postfiltering capacitor, $\mathrm{C}_{\mathrm{F}}$.

In most cases, the combined magnitudes of the dc and ac error components must be considered when selecting appropriate values for capacitors $C_{A V}$ and $C_{F}$. This combined error, representing the maximum uncertainty of the measurement, is termed the averaging error and is equal to the peak value of the output ripple plus the dc error. As the input frequency increases, both error components decrease rapidly; if the input frequency doubles, the dc error and ripple reduce to one-quarter and onehalf of their original values, respectively, and rapidly become insignificant.

## AC MEASUREMENT ACCURACY AND CREST FACTOR

The crest factor of the input waveform is often overlooked when determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms amplitude (Crest Factor $=\mathrm{V}_{\text {Peak }} / \mathrm{V}$ rms). Many common waveforms, such as sine and triangle waves, have relatively low crest factors ( $\geq 2$ ). Other waveforms, such as low duty-cycle pulse trains and SCR waveforms, have high crest factors. These types of waveforms require a long averaging time constant to average out the long time periods between pulses. Figure 10 shows the additional error vs. the crest factor of the AD737 for various values of $\mathrm{C}_{\mathrm{Av}}$.

## SELECTING PRACTICAL VALUES FOR CAPACITORS

Table 5 provides practical values of $C_{A V}$ and $C_{F}$ for several common applications.

The input coupling capacitor, $\mathrm{C}_{\mathrm{c}}$, in conjunction with the $8 \mathrm{k} \Omega$ internal input scaling resistor, determines the -3 dB low frequency roll-off. This frequency, $F_{L}$, is equal to

$$
F_{L}=\frac{1}{2 \pi(8,000)\left(\text { The Value of } C_{C} \text { in Farads }\right)}
$$

Note that at $\mathrm{F}_{\mathrm{L}}$, the amplitude error is approximately $-30 \%$ $(-3 \mathrm{~dB})$ of reading. To reduce this error to $0.5 \%$ of reading, choose a value of $\mathrm{C}_{\mathrm{C}}$ that sets $\mathrm{F}_{\mathrm{L}}$ at one-tenth of the lowest frequency to be measured.

In addition, if the input voltage has more than 100 mV of dc offset, then the ac coupling network at Pin 2 should be used in addition to capacitor Cc.

## AD737

Table 5. AD737 Capacitor Selection

| Application | RMS Input Level | Low Frequency Cutoff ( -3 dB ) | Maximum Crest Factor | Cav | $\mathrm{C}_{\mathrm{F}}$ | Settling Time ${ }^{1}$ to 1\% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| General-Purpose RMS Computation | 0-1 V | 20 Hz | 5 | $150 \mu \mathrm{~F}$ | $10 \mu \mathrm{~F}$ | 360 ms |
|  |  | 200 Hz | 5 | $15 \mu \mathrm{~F}$ | $1 \mu \mathrm{~F}$ | 36 ms |
|  | 0-200 mV | 20 Hz | 5 | $33 \mu \mathrm{~F}$ | $10 \mu \mathrm{~F}$ | 360 ms |
|  |  | 200 Hz | 5 | $3.3 \mu \mathrm{~F}$ | $1 \mu \mathrm{~F}$ | 36 ms |
| General-Purpose Average Responding | 0-1 V | 20 Hz |  | None | $33 \mu \mathrm{~F}$ | 1.2 sec |
|  |  | 200 Hz |  | None | $3.3 \mu \mathrm{~F}$ | 120 ms |
|  | 0-200 mV | 20 Hz |  | None | $33 \mu \mathrm{~F}$ | 1.2 sec |
|  |  | 200 Hz |  | None | $3.3 \mu \mathrm{~F}$ | 120 ms |
| SCR Waveform Measurement | 0-200 mV | 50 Hz | 5 | $100 \mu \mathrm{~F}$ | $33 \mu \mathrm{~F}$ | 1.2 sec |
|  |  | 60 Hz | 5 | $82 \mu \mathrm{~F}$ | $27 \mu \mathrm{~F}$ | 1.0 sec |
|  | 0-100 mV | 50 Hz | 5 | $50 \mu \mathrm{~F}$ | $33 \mu \mathrm{~F}$ | 1.2 sec |
|  |  | 60 Hz | 5 | $47 \mu \mathrm{~F}$ | $27 \mu \mathrm{~F}$ | 1.0 sec |
| Audio Applications |  |  |  |  |  |  |
| Speech | 0-200 mV | 300 Hz | 3 | $1.5 \mu \mathrm{~F}$ | $0.5 \mu \mathrm{~F}$ | 18 ms |
| Music | 0-100 mV | 20 Hz | 10 | $100 \mu \mathrm{~F}$ | $68 \mu \mathrm{~F}$ | 2.4 sec |

[^3]
## APPLICATION CIRCUITS



Figure 27. 3 1/2 Digit DVM Circuit


Figure 28. Battery-Powered Operation for 200 mV Maximum RMS Full-Scale Input


Figure 29. External Scale Factor Trim


Figure 30. dB Output Connection


Figure 31. DC-Coupled Vos and Scale Factor Trims

## OUTLINE DIMENSIONS



Figure 32. 8-Lead Standard Small Outline Package [SOIC] Narrow Body (R-8)
Dimensions shown in millimeters and (inches)
Figure 33. 8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)
Dimensions shown in inches and (millimeters)


COMPLIANT TO JEDEC STANDARDS MS-001-BA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 34. 8-Lead Plastic Dual-In-Line Package [PDIP] ( $\mathrm{N}-8$ )
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
| :---: | :---: | :---: | :---: |
| AD737AQ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-Lead Ceramic Dual In-Line Package (CERDIP) | Q-8 |
| AD737BQ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-Lead Ceramic Dual In-Line Package (CERDIP) | Q-8 |
| AD737JN | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Plastic Dual-In-Line Package (PDIP) | N-8 |
| AD737JNZ ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Plastic Dual-In-Line Package (PDIP) | N-8 |
| AD737JR | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JR-5 | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JR-5-REEL | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JR-5-REEL7 | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JR-REEL | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JR-REEL7 | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JRZ ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JRZ-5 ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JRZ-5-R71 | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JRZ-5-RL ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JRZ-R71 ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737JRZ-RL' ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737KN | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Plastic Dual-In-Line Package (PDIP) | N-8 |
| AD737KNZ ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Plastic Dual-In-Line Package (PDIP) | N-8 |
| AD737KR | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737KR-REEL | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737KR-REEL7 | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737KRZ ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737KRZ-R71 | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |
| AD737KRZ-RL ${ }^{1}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | 8-Lead Standard Small Outline Package (SOIC) Narrow Body | R-8 |

${ }^{1} \mathrm{Z}=\mathrm{Pb}$-free part.

| $\square$ | A0737 |
| :--- | :--- |

NOTES

## AD737

## NOTES


[^0]:    ${ }^{1}$ Protected under U.S. Patent Number 5,495,245.

[^1]:    One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
    Tel: 781.329.4700
    www.analog.com
    Fax: 781.326.8703 © 2005 Analog Devices, Inc. All rights reserved.

[^2]:    8-Lead PDIP package: $\theta_{\mathrm{JA}}=165^{\circ} \mathrm{C} / \mathrm{W}$.
    8 -Lead CERDIP package: $\theta_{\mathrm{JA}}=110^{\circ} \mathrm{C} / \mathrm{W}$.
    8 -Lead SOIC: $\theta_{\mathrm{JA}}=155^{\circ} \mathrm{C} / \mathrm{W}$.

[^3]:    ${ }^{1}$ Settling time is specified over the stated rms input level with the input signal increasing from zero. Settling times are greater for decreasing amplitude input signals.

