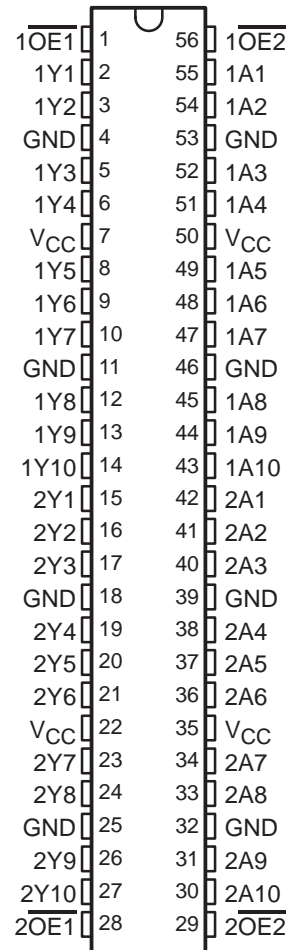


SN54ABT162827A, SN74ABT162827A 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS248F – JULY 1993 – REVISED JUNE 2004

- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- I_{off} and Power-Up 3-State Support Hot Insertion
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54ABT162827A . . . WD PACKAGE
SN74ABT162827A . . . DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

The 'ABT162827A devices are noninverting 20-bit buffers composed of two 10-bit buffers with separate output-enable signals. For either 10-bit buffer, the two output-enable ($1OE1$ and $1OE2$, or $2OE1$ and $2OE2$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------|---------------|-----------------------|-------------------|
| –40°C to 85°C | SSOP – DL | Tube | SN74ABT162827ADL | ABT162827A |
| | | Tape and reel | SN74ABT162827ADLR | |
| | TSSOP – DGG | Tape and reel | SN74ABT162827ADGGR | ABT162827A |
| –55°C to 125°C | CFP – WD | Tube | SNJ54ABT162827AWD | SNJ54ABT162827AWD |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54ABT162827A, SN74ABT162827A

20-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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description/ordering information (continued)

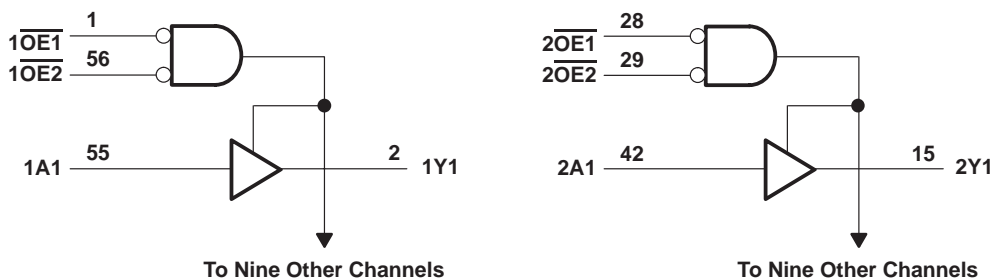
These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, \overline{OE} shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 10-bit buffer)

| INPUTS | | | OUTPUT |
|------------------|------------------|---|--------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O | 30 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DGG package | 64°C/W |
| DL package | 56°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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20-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

| | | SN54ABT162827A | | SN74ABT162827A | | UNIT |
|---------------------|------------------------------------|----------------|-----------------|----------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -3 | | -12 | mA |
| I _{OL} | Low-level output current | | 8 | | 12 | mA |
| Δt/ΔV | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| Δt/ΔV _{CC} | Power-up ramp rate | 200 | | 200 | | μs/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT162827A, SN74ABT162827A

20-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A = 25°C | | | SN54ABT162827A | | SN74ABT162827A | | UNIT | |
|--------------------|--|---|------------------|------|----------------|------|----------------|------|------|----|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | -1.2 | | -1.2 | V | |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -1 mA | 3.35 | | | 3.35 | | 3.35 | | V | |
| | V _{CC} = 5 V, I _{OH} = -1 mA | 3.85 | | | 3.85 | | 3.85 | | | |
| | V _{CC} = 4.5 V | | 3.1 | | 3.1 | | 3.1 | | | |
| V _{OL} | V _{CC} = 4.5 V | | | 0.4 | | 0.8 | | 0.65 | V | |
| | | | | | | 0.8* | | 0.8 | | |
| V _{hys} | | | 100 | | | | | | mV | |
| I _I | V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND | | | ±1 | | ±1 | | ±1 | µA | |
| I _{OZPU} | V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | | | ±50 | | ±50 | | ±50 | µA | |
| I _{OZPD} | V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | | | ±50 | | ±50 | | ±50 | µA | |
| I _{OZH} ‡ | V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V | | | 10 | | 10 | | 10 | µA | |
| I _{OZL} ‡ | V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V | | | -10 | | -10 | | -10 | µA | |
| I _{off} | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | | ±100 | | | | ±100 | µA | |
| I _{CEX} | V _{CC} = 5.5 V, V _O = 5.5 V | | | 50 | | 50 | | 50 | µA | |
| I _O § | V _{CC} = 5.5 V, V _O = 2.5 V | -25 | -75 | -100 | -25 | -100 | -25 | -100 | mA | |
| I _{CC} | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | 2 | | 2 | | 2 | mA | |
| | | Outputs low | | 32 | | 32 | | 32 | | |
| | | Outputs disabled | | 2 | | 2 | | 2 | | |
| ΔI _{CC} ¶ | Data inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | Outputs enabled | | 1 | | 1.5 | | 1 | mA |
| | | | Outputs disabled | | 0.05 | | 1 | | 0.05 | |
| | Control inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | | 1.5 | | 1.5 | | 1.5 | | |
| C _i | V _I = 2.5 V or 0.5 V | | | 4 | | | | | pF | |
| C _o | V _O = 2.5 V or 0.5 V | | | 7 | | | | | pF | |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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SN54ABT162827A, SN74ABT162827A
20-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25^\circ$ C | | | SN54ABT162827A | | SN74ABT162827A | | UNIT |
|-----------|-----------------|----------------|---------------------------------------|-----|-----|----------------|-----|----------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1 | 2.1 | 3.6 | 1 | 4.1 | 1 | 3.9 | ns |
| t_{PHL} | | | 1.1 | 2.8 | 4.2 | 1.1 | 5 | 1.1 | 4.7 | |
| t_{PZH} | \overline{OE} | Y | 1.5 | 3.4 | 6.3 | 1.5 | 7.2 | 1.5 | 6.9 | ns |
| t_{PZL} | | | 1.6 | 3.5 | 5.3 | 1.6 | 6.6 | 1.6 | 6.3 | |
| t_{PHZ} | \overline{OE} | Y | 2.1 | 4.1 | 6.5 | 2.1 | 6.8 | 2.1 | 6.6 | ns |
| t_{PLZ} | | | 1.5 | 3.5 | 5.9 | 1.5 | 7.3 | 1.5 | 6.3 | |

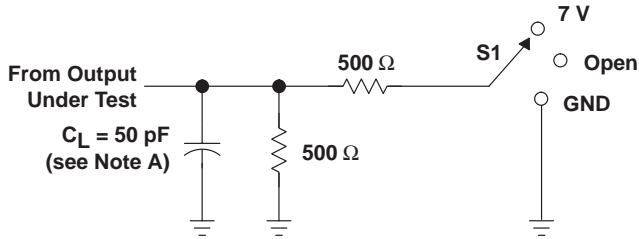
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SN54ABT162827A, SN74ABT162827A
20-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

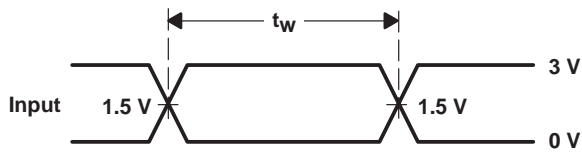
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PARAMETER MEASUREMENT INFORMATION

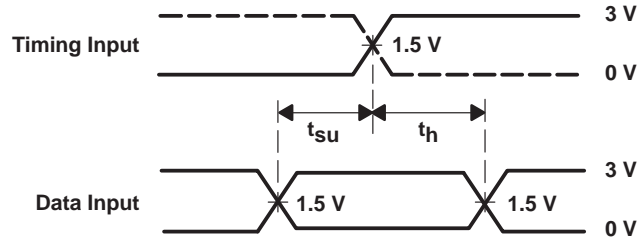


LOAD CIRCUIT

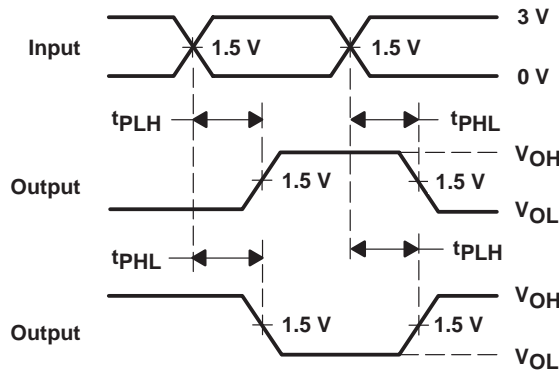
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



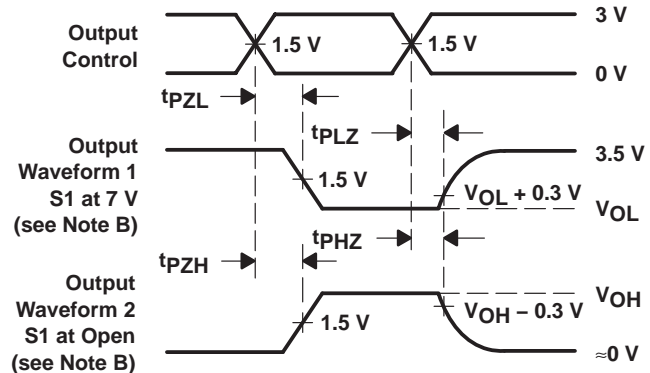
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74ABT162827ADGGRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ABT162827ADGGRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ABT162827ADLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT162827ADGGR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT162827ADL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT162827ADLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT162827ADLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT162827ADGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74ABT162827ADLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT162827ADGGR | TSSOP | DGG | 56 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ABT162827ADLR | SSOP | DL | 56 | 1000 | 346.0 | 346.0 | 49.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

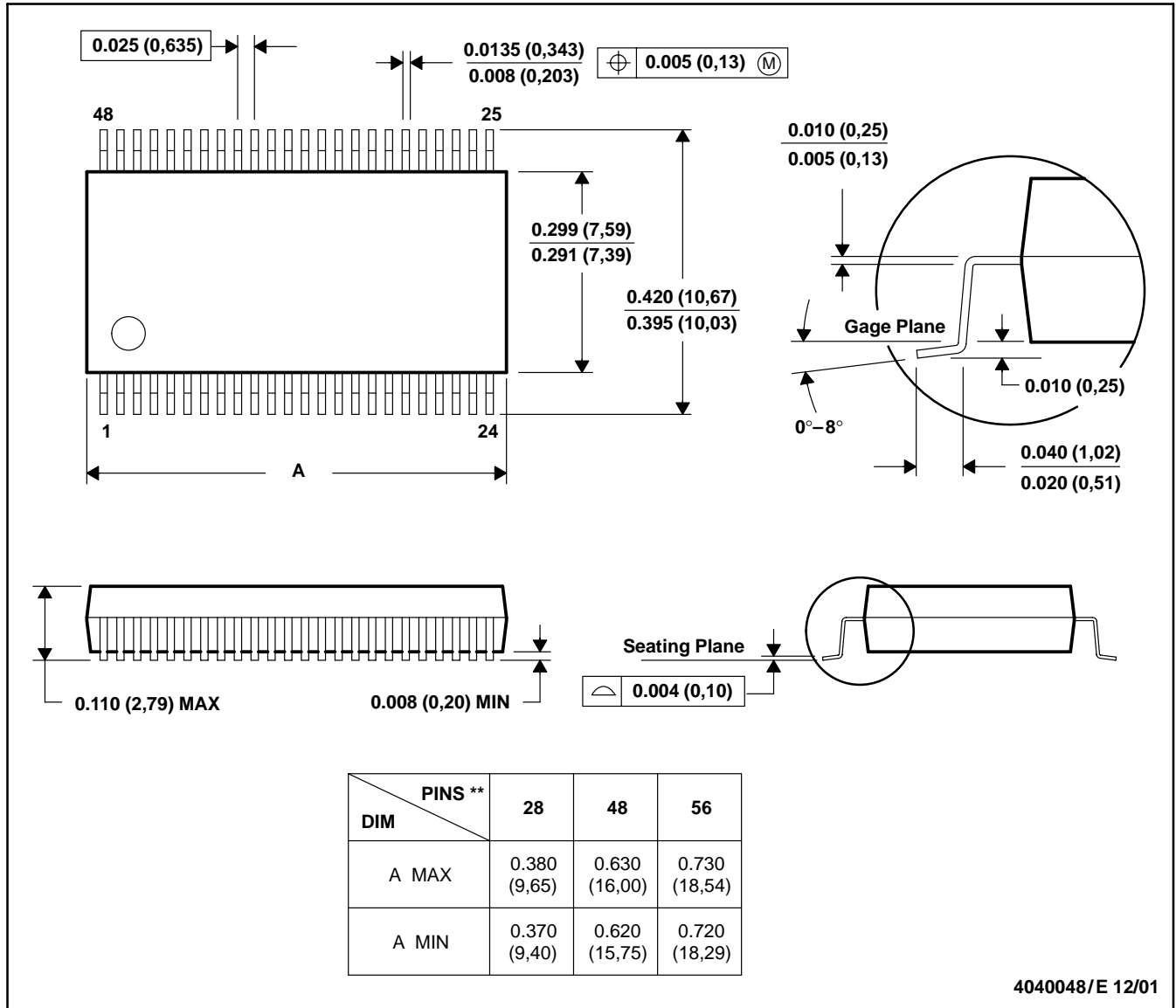


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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