



NDT2955

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P-Channel Enhancement Mode Field Effect Transistor

General Description

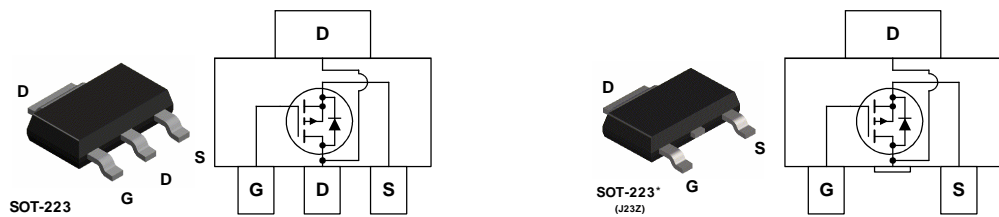
This 60V P-Channel MOSFET is produced using Fairchild Semiconductor's high voltage Trench process. It has been optimized for power management applications.

Applications

- DC/DC converter
- Power management

Features

- -2.5 A, -60 V. $R_{DS(ON)} = 300m\Omega @ V_{GS} = -10 V$
 $R_{DS(ON)} = 500m\Omega @ V_{GS} = -4.5 V$
- High density cell design for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package.



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-60	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current – Continuous (Note 1a)	-2.5	A
	– Pulsed	-15	
P _D	Maximum Power Dissipation (Note 1a) (Note 1b) (Note 1c)	3.0	W
		1.3	
		1.1	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	12	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2955	NDT2955	13"	12mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Avalanche Ratings

W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 30\text{ V}$, $I_D = 2.5\text{ A}$			174	mJ
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = -250\ \mu\text{A}$	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-60		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -60\text{ V}$, $V_{GS} = 0\text{ V}$			-10	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-2	-2.6	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		5.7		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}$, $I_D = -2.5\text{ A}$ $V_{GS} = -4.5\text{ V}$, $I_D = -2\text{ A}$ $V_{GS} = -10\text{ V}$, $I_D = -2.5\text{ A}$, $T_J = 125^\circ\text{C}$		95 163 153	300 500 513	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}$, $V_{DS} = -5\text{ V}$	-12			A
g_{FS}	Forward Transconductance	$V_{DS} = -10\text{ V}$, $I_D = -2.5\text{ A}$		5.5		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -30\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		601		pF
C_{oss}	Output Capacitance			85		pF
C_{rss}	Reverse Transfer Capacitance			35		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30\text{ V}$, $I_D = -1\text{ A}$, $V_{GS} = -10\text{ V}$, $R_{GEN} = 6\ \Omega$		12	21	ns
t_r	Turn-On Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			19	34	ns
t_f	Turn-Off Fall Time			6	12	ns
Q_g	Total Gate Charge	$V_{DS} = -30\text{ V}$, $I_D = -2.5\text{ A}$, $V_{GS} = -10\text{ V}$		11	15	nC
Q_{gs}	Gate-Source Charge			2.4		nC
Q_{gd}	Gate-Drain Charge			2.7		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current			-2.5	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -2.5\text{ A}$ (Note 2)		-0.8	-1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -2.5\text{ A}$, $d_i/d_t = 100\text{ A}/\mu\text{s}$		25		nS
Q_{rr}	Diode Reverse Recovery Charge			40		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $42^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $95^\circ\text{C}/\text{W}$ when mounted on a $.0066\text{ in}^2$ pad of 2 oz copper



c) $110^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

2. Pulse Test: Pulse Width < $300\ \mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics

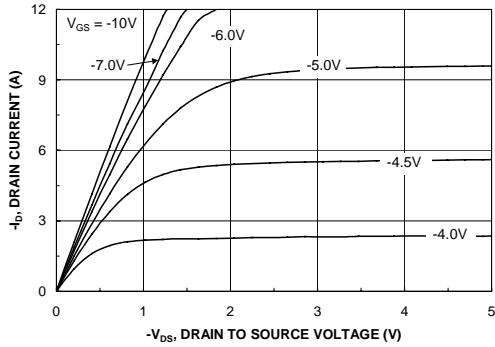


Figure 1. On-Region Characteristics.

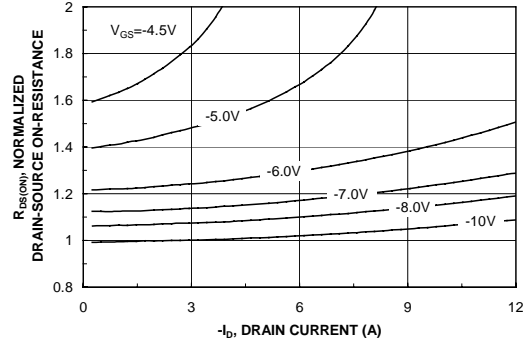


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

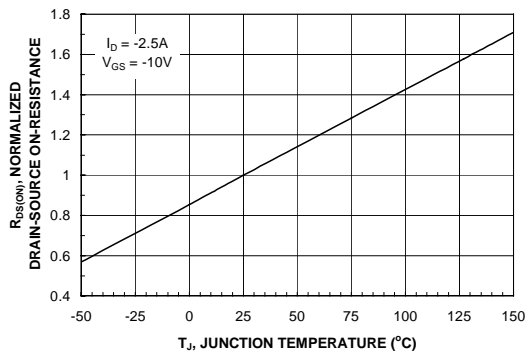


Figure 3. On-Resistance Variation with Temperature.

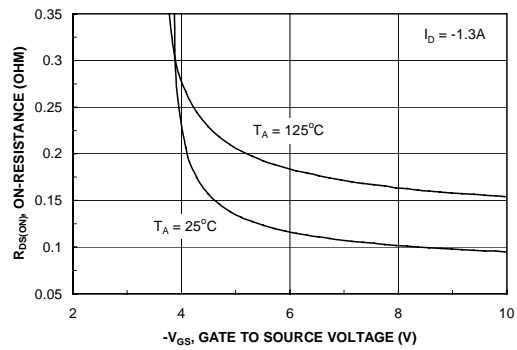


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

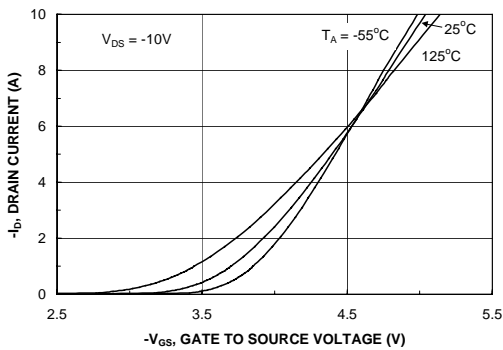


Figure 5. Transfer Characteristics.

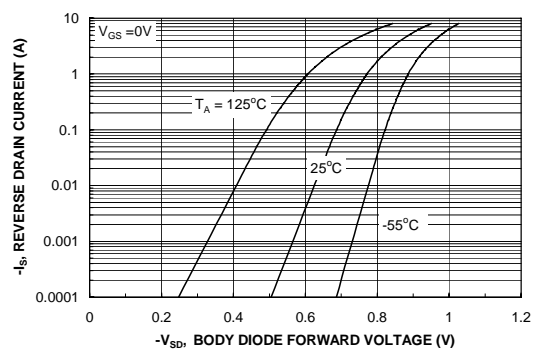
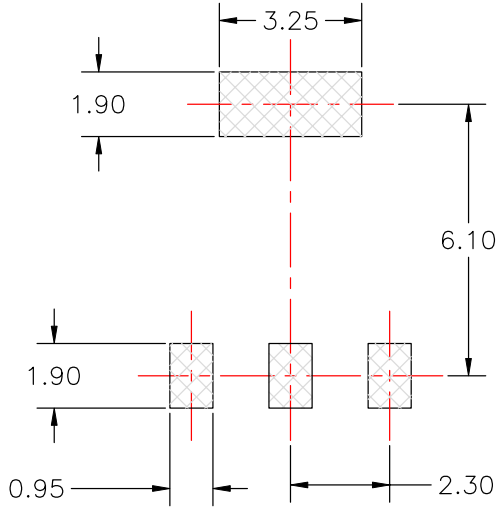
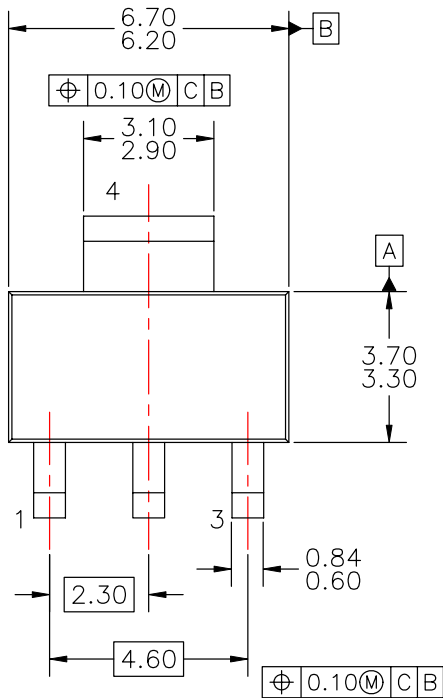


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

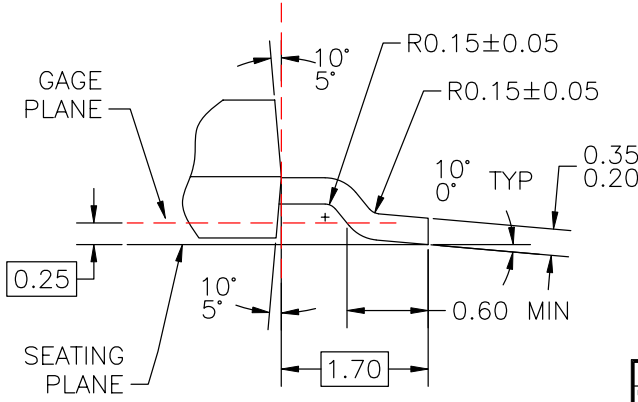
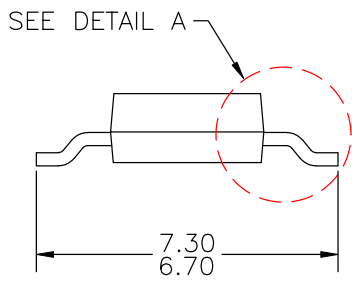
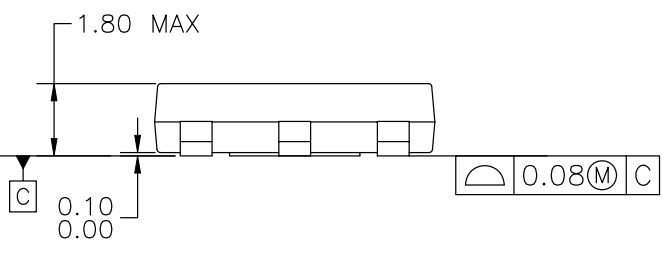
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APPROVED
July-14-2008

REVISIONS			
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR 0.74 ±0.03 TO 0.60-0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR 1.8 ±0.05 TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR 0.35 ±0.03 TO 0.20-0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR 3.56 ±0.33 TO 3.3; CHG BODY LN FR 6.53 ±0.33 TO 6.3; CHG TOTAL PKG WID FR 6.94 ±0.33 TO 7.3; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP



LAND PATTERN RECOMMENDATION



DETAIL A
SCALE: 2:1

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING BASED ON JEDEC REGISTRATION TO-261, VARIATION AA.
 - B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - C) ALL DIMENSIONS ARE IN MILLIMETERS.
 - D) DRAWING CONFORMS TO ASME Y14.5M-1994.
 - E) LANDPATTERN NAME: SOT230P700X180-4BN
 - F) DRAWING FILENAME: MKT-MA04AREV2

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™		
DRAWN: J.U. COMPARATIVO JR.	26FEB2008			
CHECKED: L.Z. STA CRUZ				
APPROVED: M.R. GESTOLE				
G.S. BAJE		MOLDED PACKAGE SOT-223, 4 LEAD		
PROJECTION 	SCALE 1:1	SIZE A3	DRAWING NUMBER MKT-MA04A	REV 2
	FORMERLY: N/A			SHEET : 1 OF 1



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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