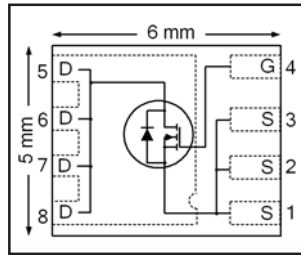


HEXFET® Power MOSFET

### Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- PWM Inverterized topologies
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters



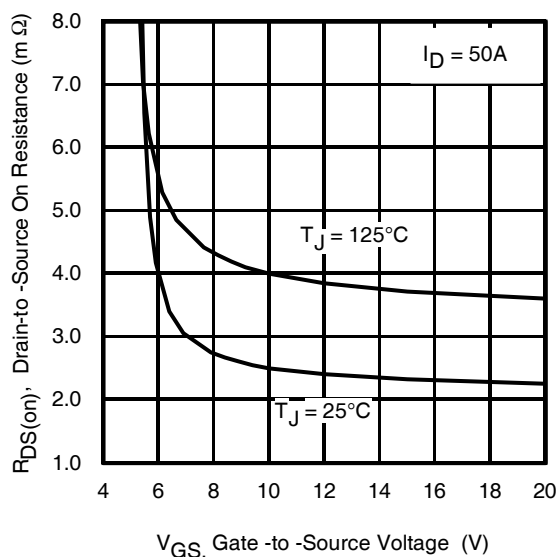
<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ. max.</b>	<b>2.5mΩ</b>
	<b>3.3mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>117A</b> Ⓢ
<b>I<sub>D</sub> (Package Limited)</b>	<b>85A</b>

### Benefits

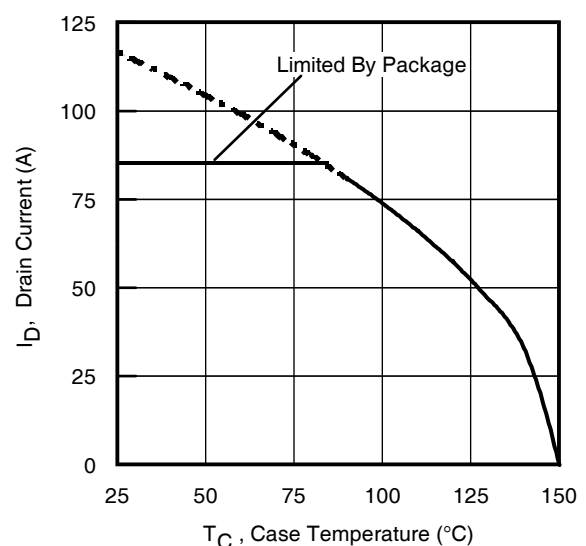
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- RoHS Compliant containing no Lead, no Bromide, and no Halogen



Base Part Number	Package Type	Standard Pack		Orderable part number	Note
		Form	Quantity		
IRFH7446PbF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH7446TRPbF	
	PQFN 5mm x 6mm	Tape and Reel	400	IRFH7446TR2PbF	EOL notice #259



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	117 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	74 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	85	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	468	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	78	W
	Linear Derating Factor	0.63	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	78	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value <sup>④</sup>	153	
$I_{AR}$	Avalanche Current <sup>②</sup>	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>②</sup>		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case <sup>⑤</sup>	—	1.6	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case <sup>⑤</sup>	—	31	
$R_{\theta JA}$	Junction-to-Ambient <sup>⑥</sup>	—	35	
$R_{\theta JA} (<10\text{s})$	Junction-to-Ambient <sup>⑥</sup>	—	23	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1.0\text{mA}$ <sup>⑦</sup>
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.5	3.3	mΩ	$V_{GS} = 10\text{V}$ , $I_D = 50\text{A}$ <sup>⑧</sup>
		—	3.8	—	mΩ	$V_{GS} = 6.0\text{V}$ , $I_D = 50\text{A}$ <sup>⑧</sup>
$V_{GS(th)}$	Gate Threshold Voltage	2.2	—	3.9	V	$V_{DS} = V_{GS}$ , $I_D = 100\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Internal Gate Resistance	—	1.5	—	Ω	

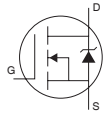
**Notes:**

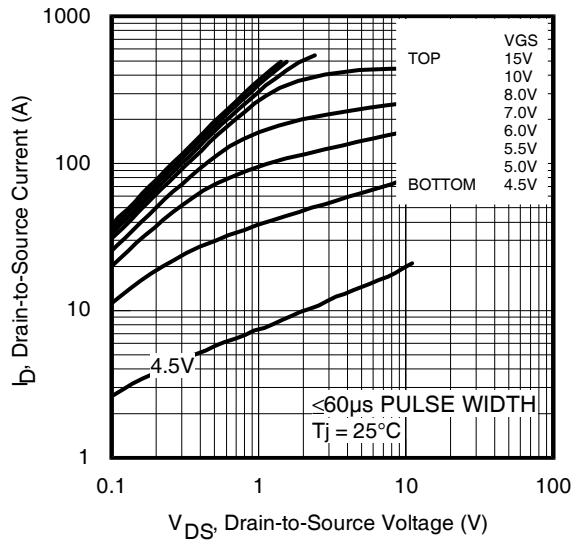
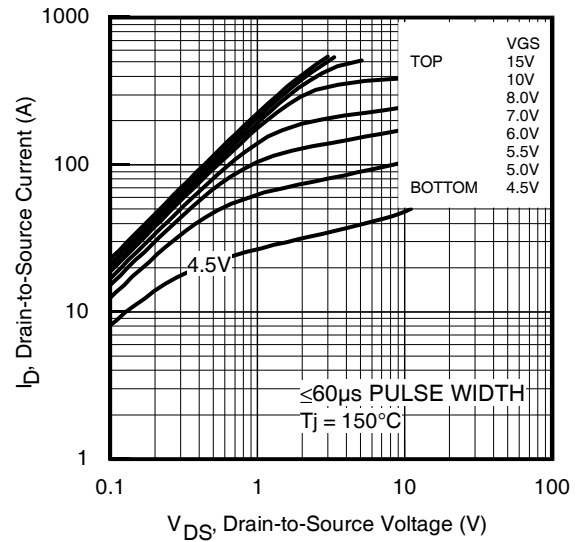
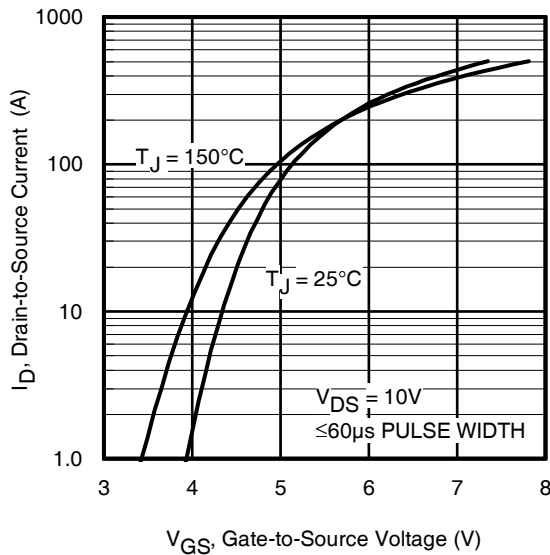
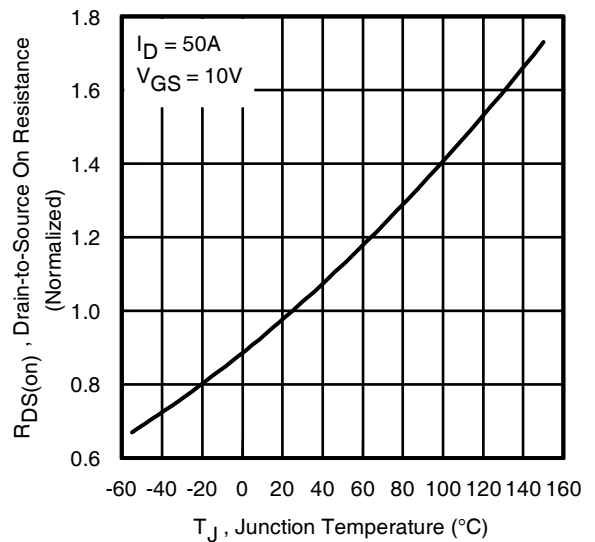
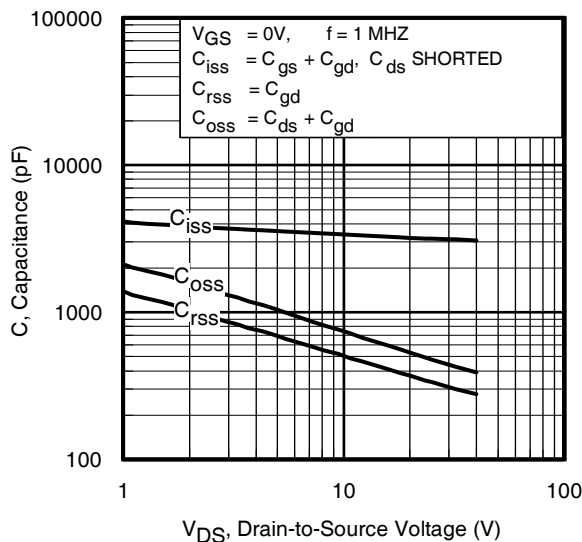
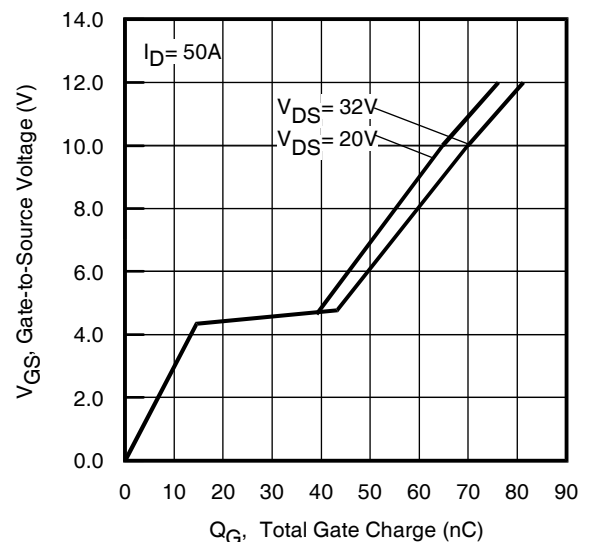
- ① Calculated continuous current based on maximum allowable junction temperature. Current is limited to 71A by source bond technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.062\text{mH}$   
 $R_G = 50\Omega$ ,  $I_{AS} = 50\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ④  $I_{SD} \leq 50\text{A}$ ,  $di/dt \leq 1123\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧ When mounted on 1 inch square 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.
- ⑨  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑩ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.062\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 50\text{A}$ ,  $V_{GS} = 10\text{V}$ .

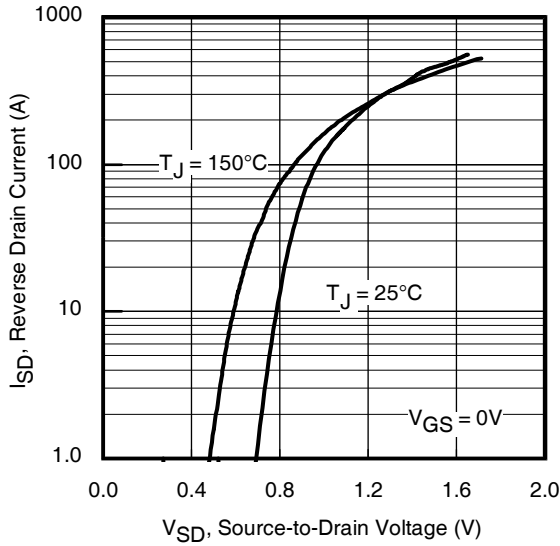
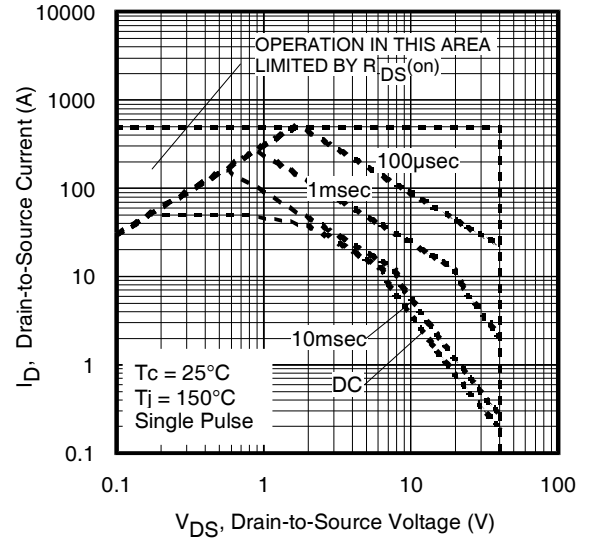
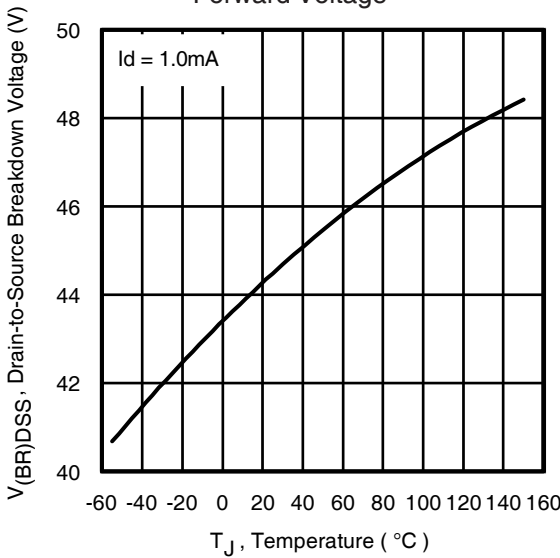
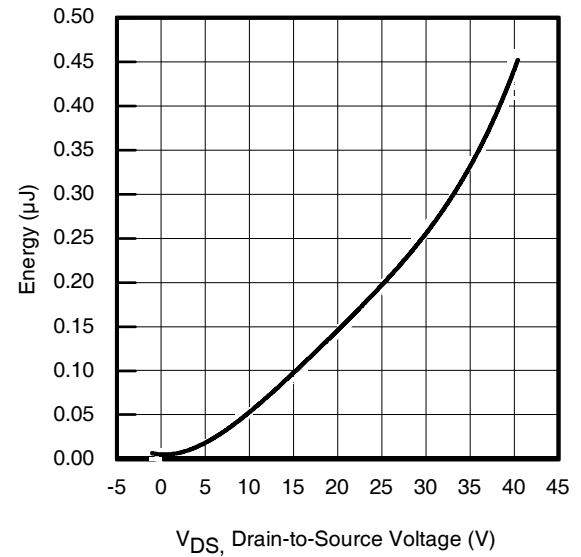
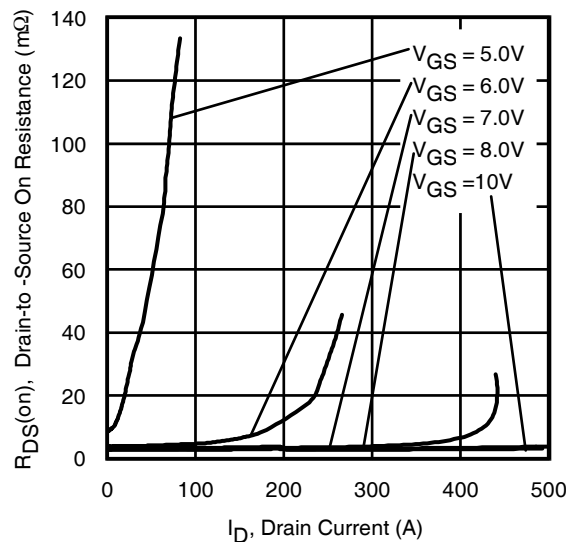
**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

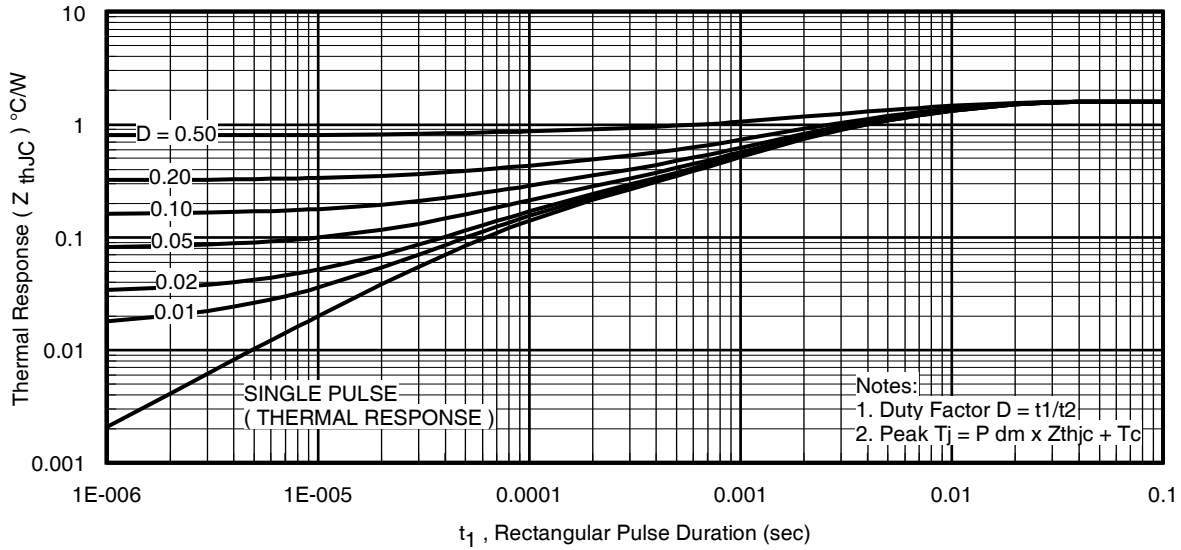
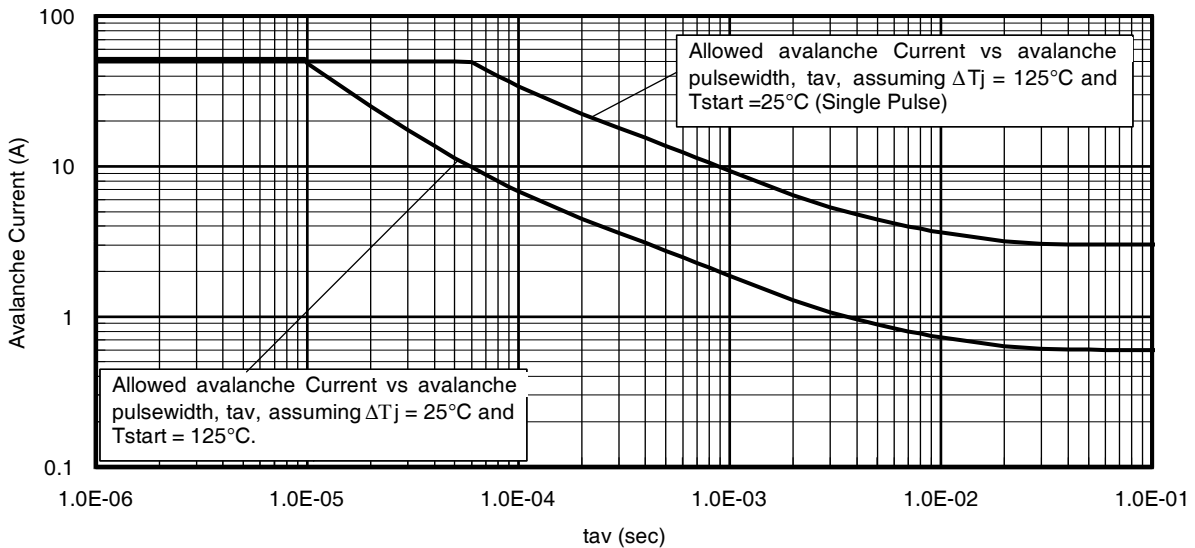
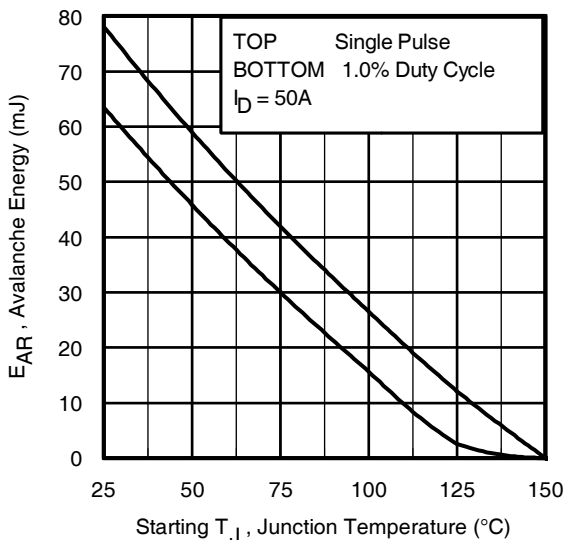
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	159	—	—	S	$V_{DS} = 10\text{V}, I_D = 50\text{A}$
$Q_g$	Total Gate Charge	—	65	98	nC	$I_D = 50\text{A}$ $V_{DS} = 20\text{V}$ $V_{GS} = 10\text{V}$ ⑤
$Q_{gs}$	Gate-to-Source Charge	—	16	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	23	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	42	—		
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 20\text{V}$ $I_D = 30\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ⑤
$t_r$	Rise Time	—	37	—		
$t_{d(off)}$	Turn-Off Delay Time	—	33	—		
$t_f$	Fall Time	—	26	—		
$C_{iss}$	Input Capacitance	—	3174	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$ $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 32\text{V}$ ⑦ $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 32\text{V}$ ⑥
$C_{oss}$	Output Capacitance	—	479	—		
$C_{rss}$	Reverse Transfer Capacitance	—	332	—		
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	637	—		
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	656	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	85 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ②	—	—	468	A	
$V_{SD}$	Diode Forward Voltage	—	0.9	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50\text{A}, V_{GS} = 0\text{V}$ ③
$dv/dt$	Peak Diode Recovery ④	—	2.6	—	V/ns	$T_J = 150^\circ\text{C}, I_S = 50\text{A}, V_{DS} = 40\text{V}$
$t_{rr}$	Reverse Recovery Time	—	16	—	ns	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $V_R = 34\text{V},$ $I_F = 50\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ ③
		—	18	—		
$Q_{rr}$	Reverse Recovery Charge	—	5.0	—	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
		—	6.9	—		
$I_{RRM}$	Reverse Recovery Current	—	0.50	—	A	$T_J = 25^\circ\text{C}$


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{OSS}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current

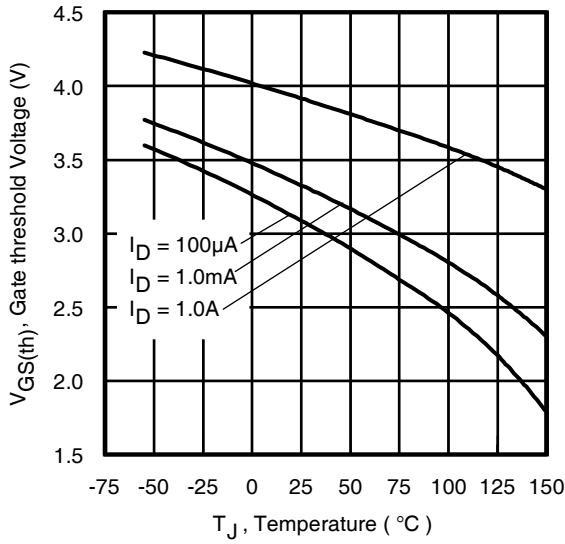
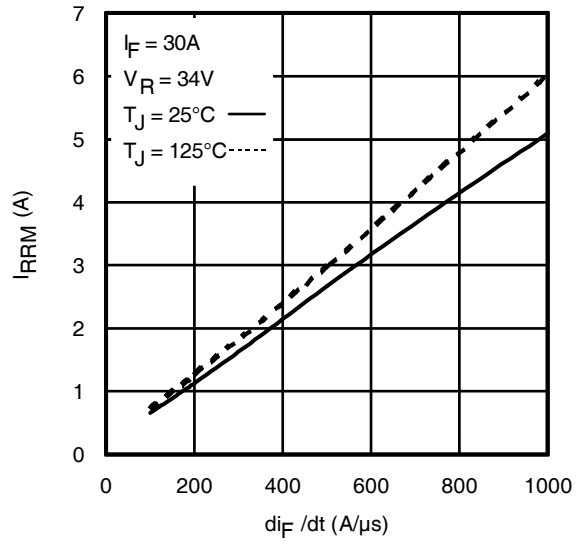
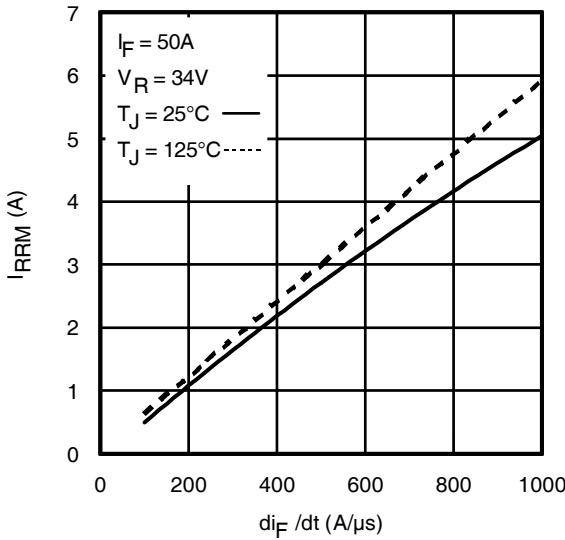
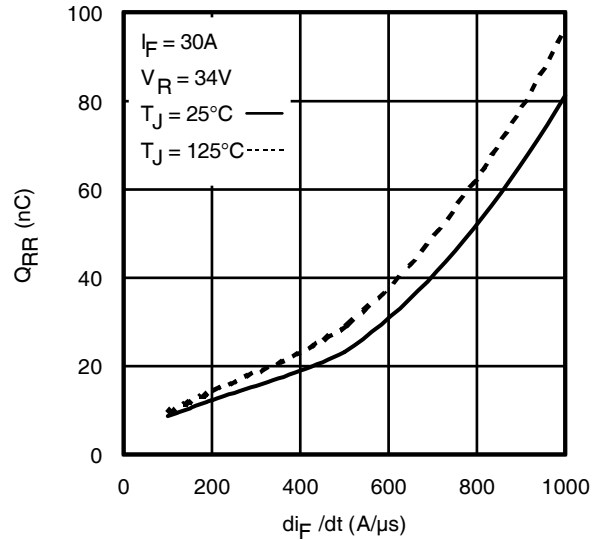
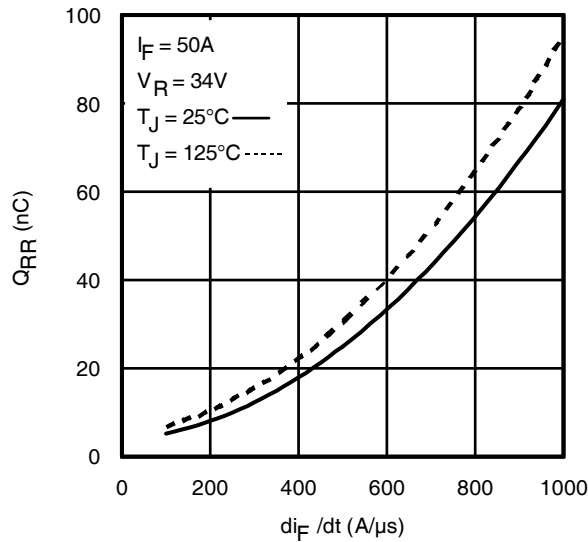

**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Typical Avalanche Current vs. Pulsewidth**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at www.irf.com)**

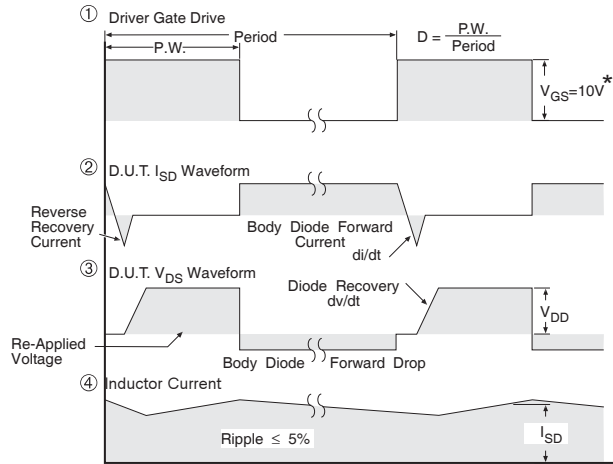
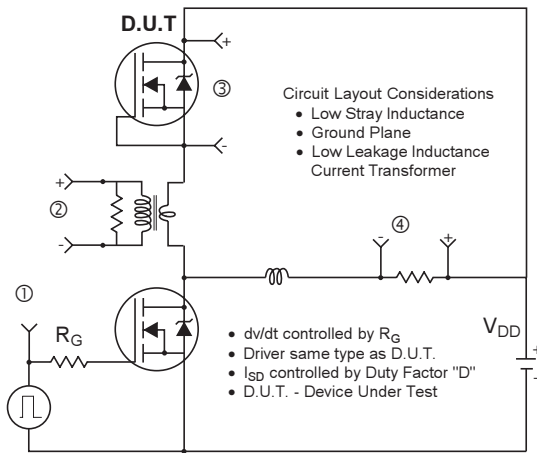
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

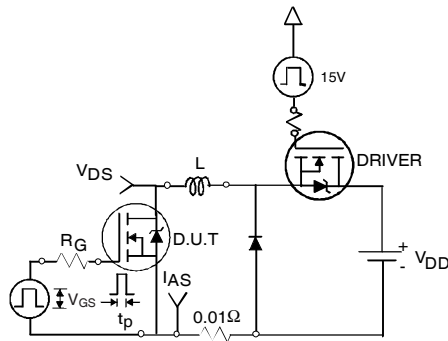
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


**Fig 17. Threshold Voltage vs. Temperature**

**Fig. 18 - Typical Recovery Current vs.  $di_f/dt$** 

**Fig. 19 - Typical Recovery Current vs.  $di_f/dt$** 

**Fig. 20 - Typical Stored Charge vs.  $di_f/dt$** 

**Fig. 21 - Typical Stored Charge vs.  $di_f/dt$**

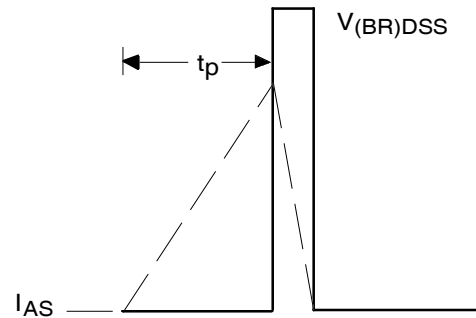


\*  $V_{GS} = 5V$  for Logic Level Devices

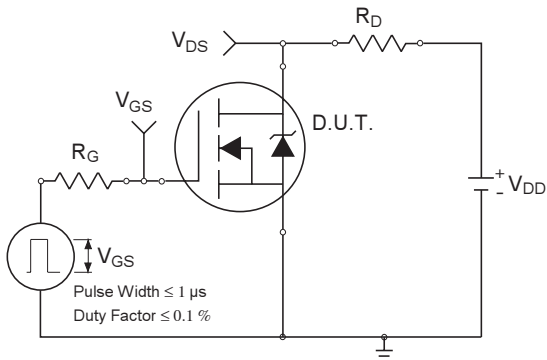
**Fig 22. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



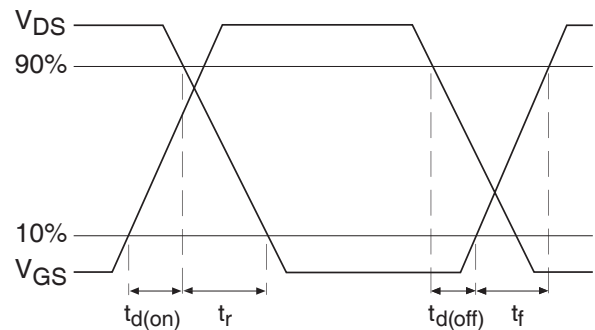
**Fig 22a. Unclamped Inductive Test Circuit**



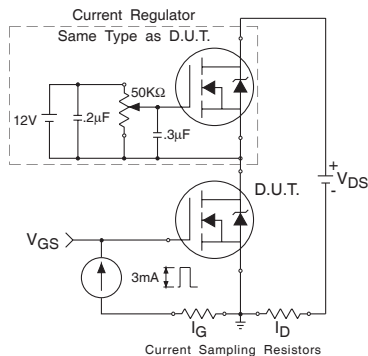
**Fig 22b. Unclamped Inductive Waveforms**



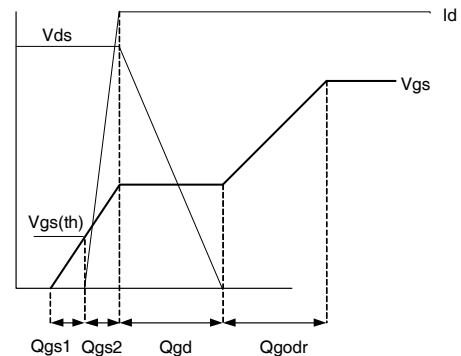
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



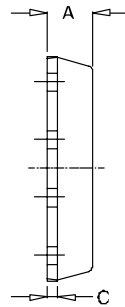
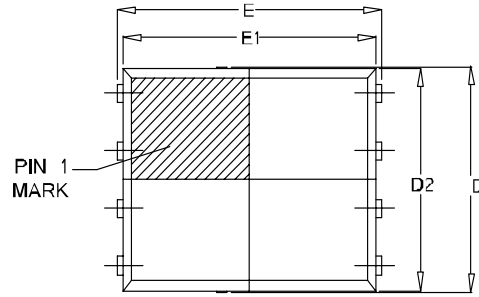
**Fig 24a. Gate Charge Test Circuit**



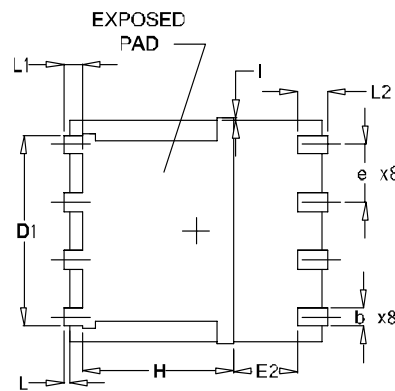
**Fig 24b. Gate Charge Waveform**



## PQFN 5x6 Outline "E" Package Details


**SIDEVIEW**

**TOP VIEW**

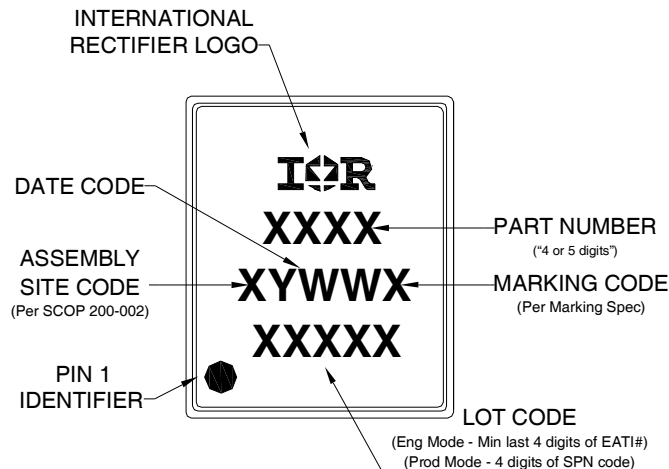
SYMBOL	OUTLINE PQFN 5X6E		
	MIN.	NOM	MAX.
A	0.90	1.03	1.17
b	0.33	0.41	0.48
C	0.20	0.25	0.35
D	4.80	4.98	5.15
D1	3.91	4.11	4.31
D2	4.80	4.90	5.00
E	5.90	6.02	6.15
E1	5.65	5.75	5.85
E2	1.10	—	—
e	1.27 BSC		
L	0.05	0.15	0.25
L1	0.38	0.44	0.50
L2	0.51	0.68	0.86
H	3.32	3.45	3.58
I	—	—	0.18


**BOTTOM VIEW**

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

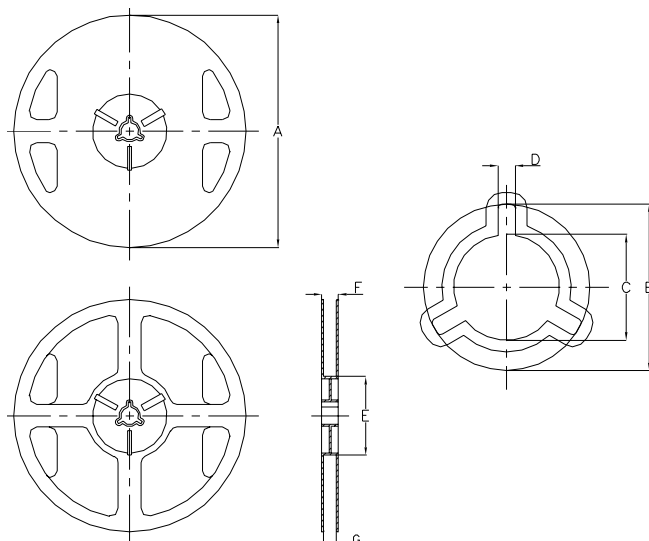
For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

## PQFN 5x6 Outline "E" Part Marking



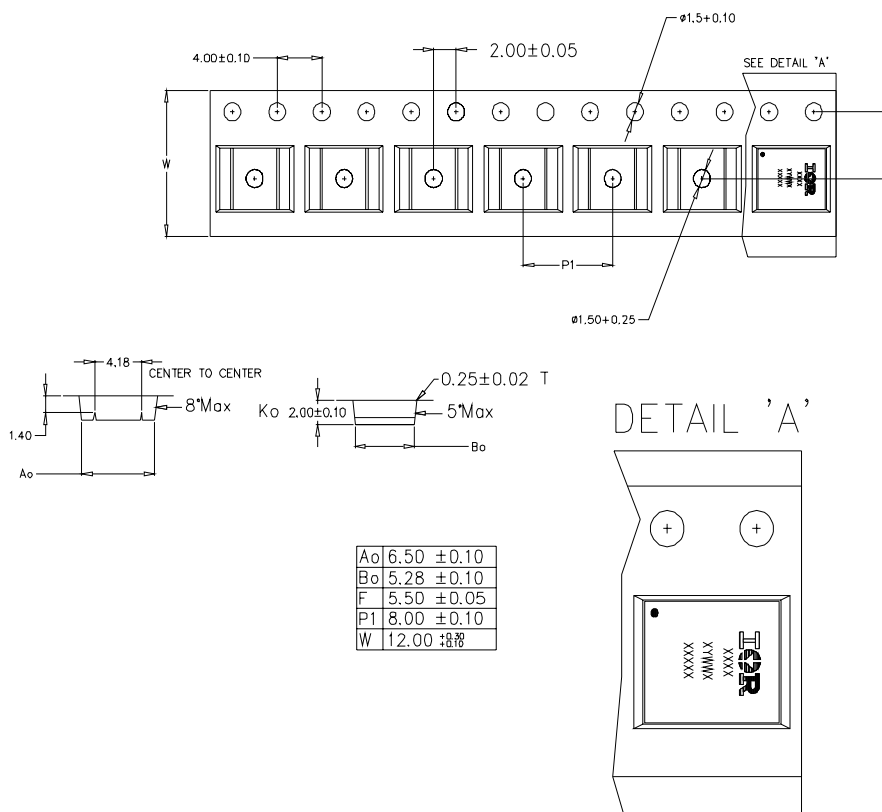
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

# PQFN 5x6 Outline "E" Tape and Reel



NOTE: Controlling dimensions in mm Std reel quantity is 4000 parts.

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4000)				TR1 OPTION (QTY 400)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
A	329.5	330.5	12.972	13.011	177.5	178.5	6.988	7.028
B	20.9	21.5	0.823	0.846	20.9	21.5	0.823	0.846
C	12.8	13.5	0.504	0.532	13.2	13.8	0.520	0.543
D	1.7	2.3	0.067	0.091	1.9	2.3	0.075	0.091
E	97	99	3.819	3.898	65	66	2.350	2.598
F	Ref	17.4			Ref	12		
G	13	14.5	0.512	0.571	13	14.5	0.512	0.571



**Qualification information<sup>†</sup>**

Qualification level	Industrial (per JEDEC JES D47F guidelines) <sup>††</sup>	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comment
1/17/2014	• Updated ordering information to reflect the End-Of-Life (EOL) of the mini-reel option (EOL notice #259).



**IR WORLD HEADQUARTERS:** 101 N. Sepulveda Blvd., El Segundo, California 90245, USA  
 To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>