

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™ 5 Power-Transistor, 100 V
IPA083N10N5

Data Sheet

Rev. 2.0
Final

1 Description

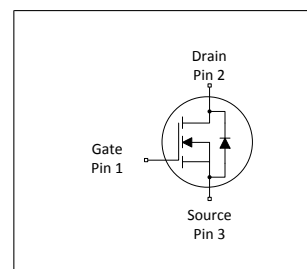
Features

- Ideal for high frequency switching and sync. rec.
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Halogen-free according to IEC61249-2-21



Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	8.3	mΩ
I_D	44	A
Q_{oss}	40	nC
$Q_G(0V..10V)$	30	nC



Type / Ordering Code	Package	Marking	Related Links
IPA083N10N5	PG-TO220-FP	083N10N5	-

¹⁾ J-STD20 and JESD22

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	44 32	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	176	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	70	mJ	$I_D=44\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	36	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	3.1	4.1	K/W	-

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=49\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	7.2 8.8	8.3 11.0	m Ω	$V_{GS}=10\text{ V}$, $I_D=44\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=22\text{ A}$
Gate resistance ²⁾	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	38	76	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=44\text{ A}$

¹⁾ see figure 3

²⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2100	2730	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	337	438	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	16	28	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=44\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Rise time	t_r	-	5	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=44\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	24	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=44\text{ A}$, $R_{G,ext}=1.6\ \Omega$
Fall time	t_f	-	5	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=44\text{ A}$, $R_{G,ext}=1.6\ \Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10	-	nC	$V_{DD}=50\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	6	10	nC	$V_{DD}=50\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	10	-	nC	$V_{DD}=50\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	30	37	nC	$V_{DD}=50\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	$V_{DD}=50\text{ V}$, $I_D=44\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	40	53	nC	$V_{DD}=50\text{ V}$, $V_{GS}=0\text{ V}$

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	30	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	176	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=44\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	55	110	ns	$V_R=50\text{ V}$, $I_F=I_S$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	95	190	nC	$V_R=50\text{ V}$, $I_F=I_S$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

5 Electrical characteristics diagrams

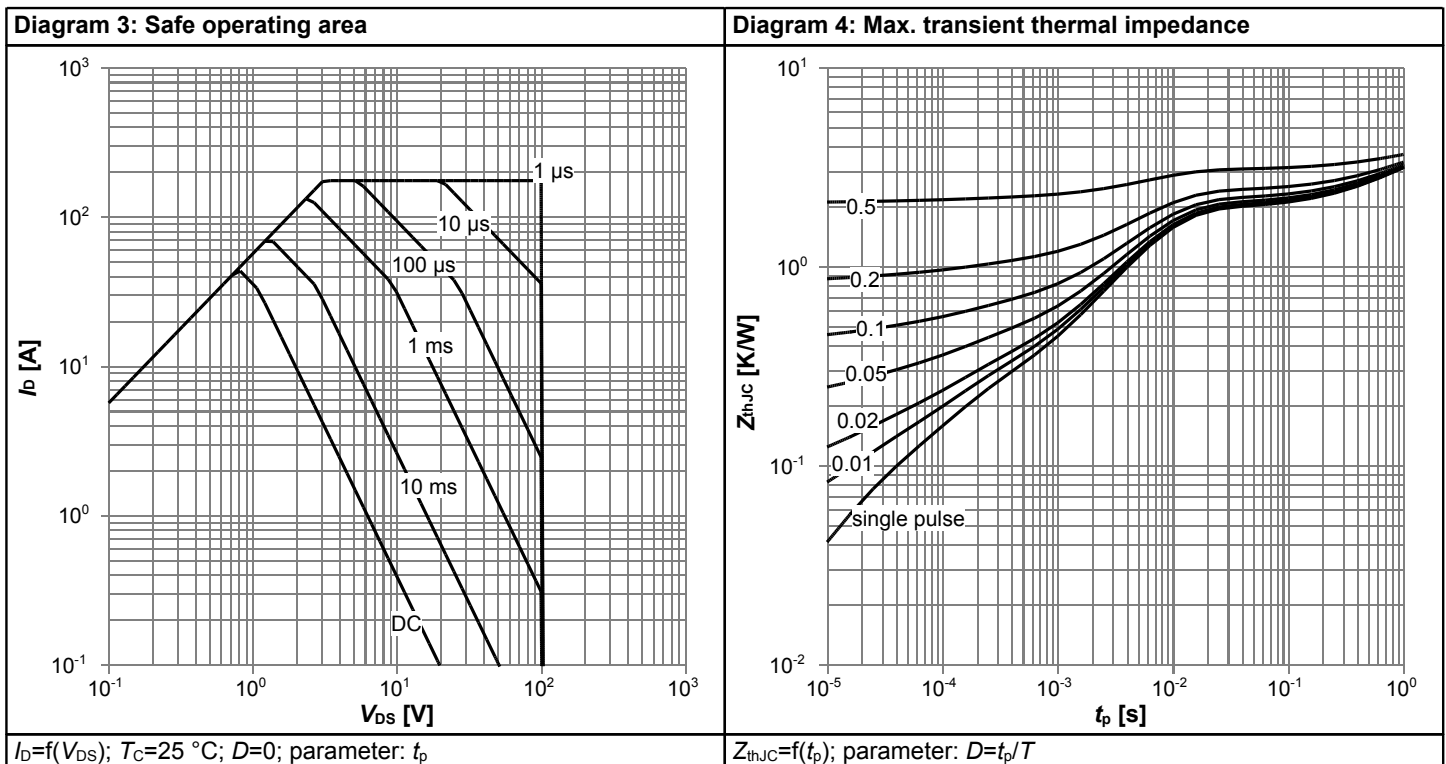
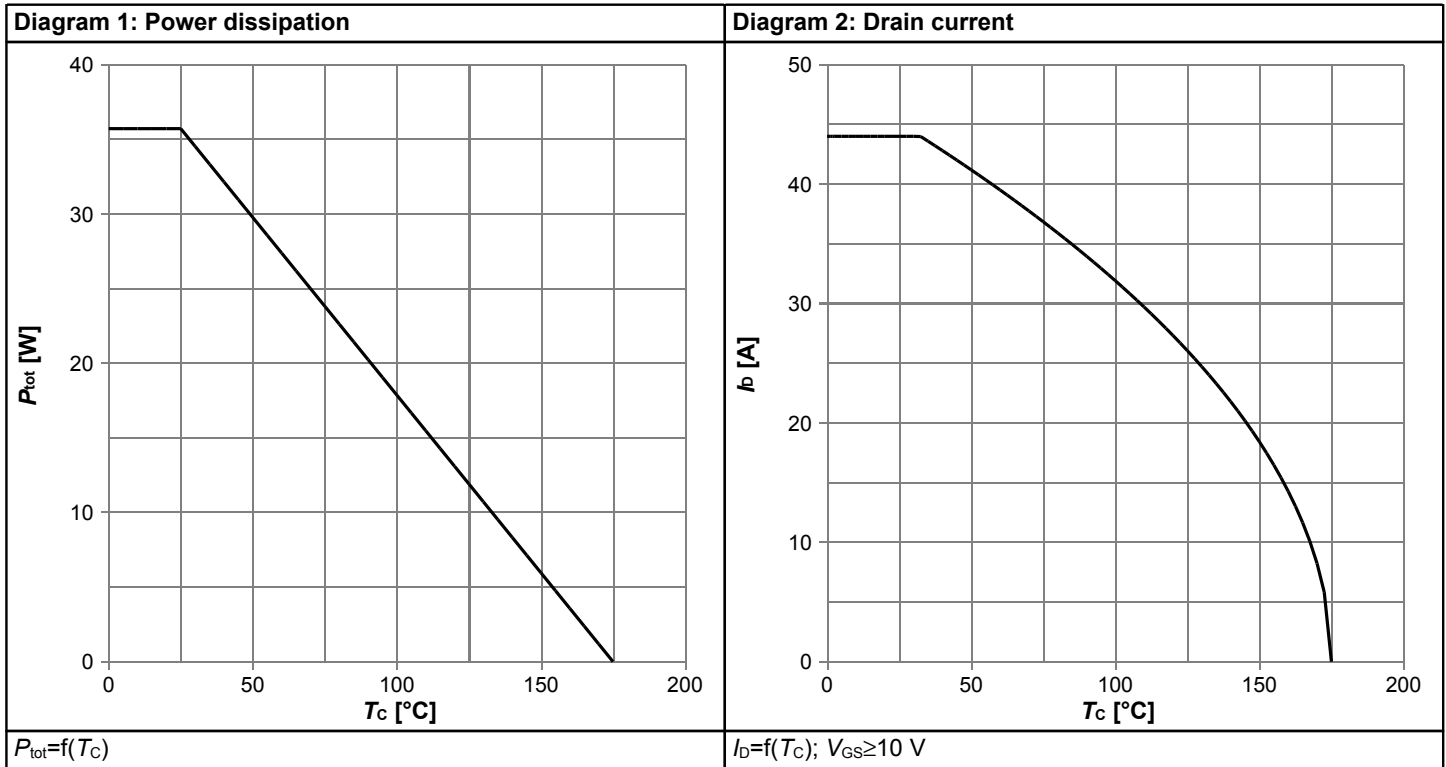
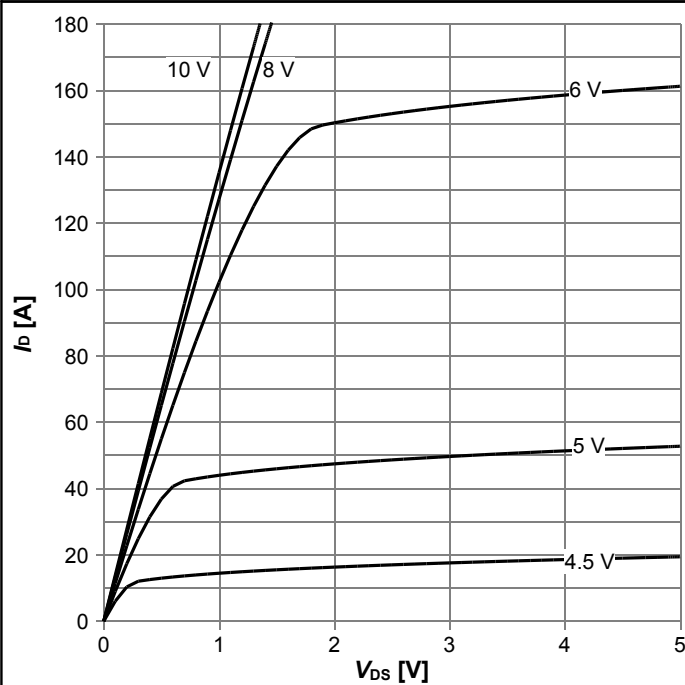
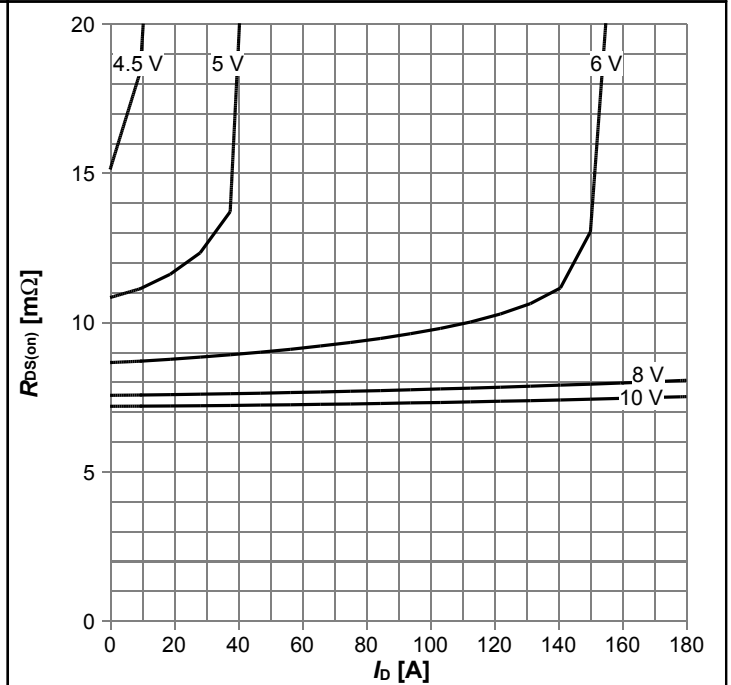


Diagram 5: Typ. output characteristics



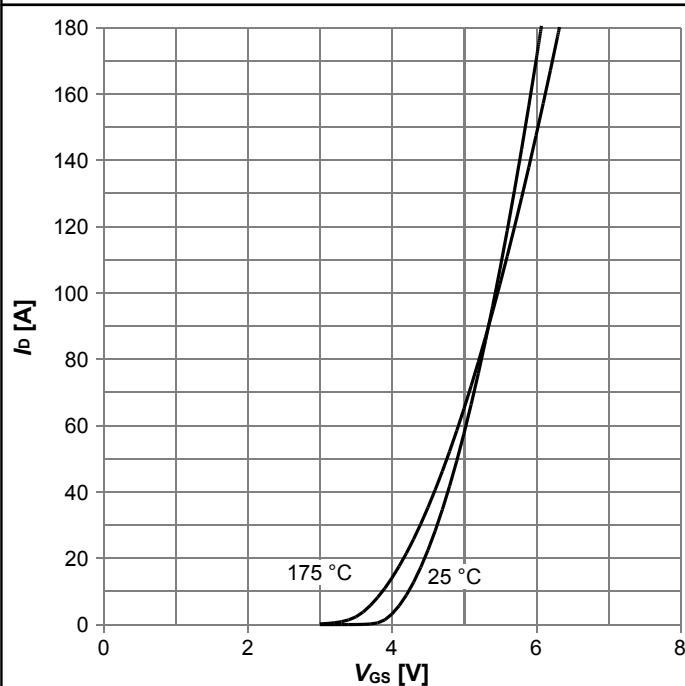
$I_D=f(V_{DS})$; $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



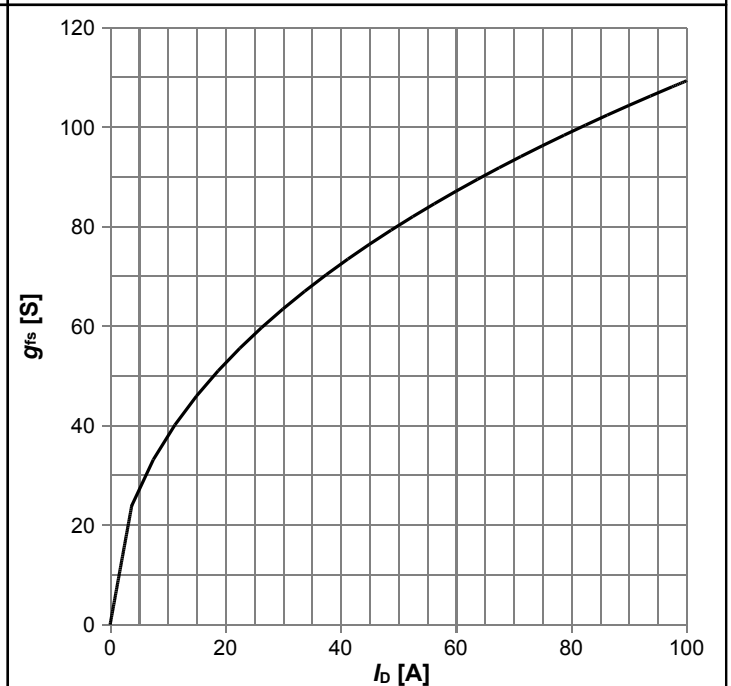
$R_{DS(on)}=f(I_D)$; $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



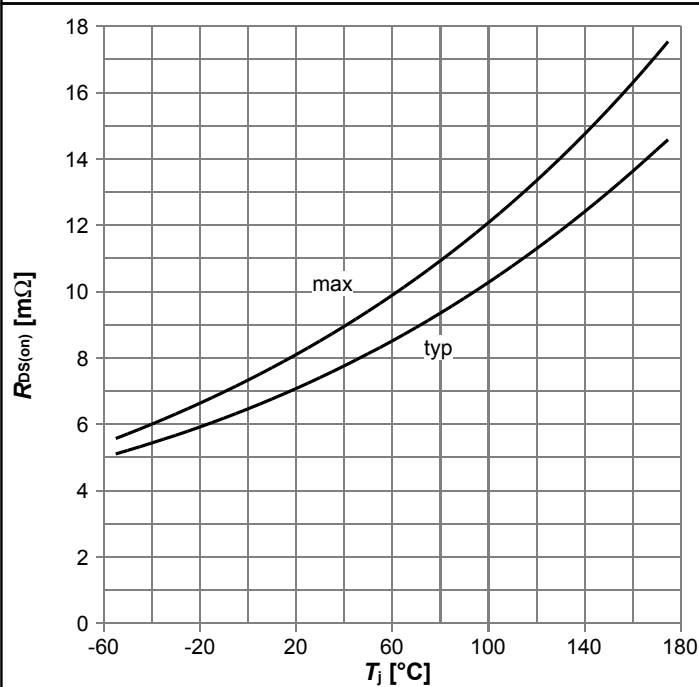
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



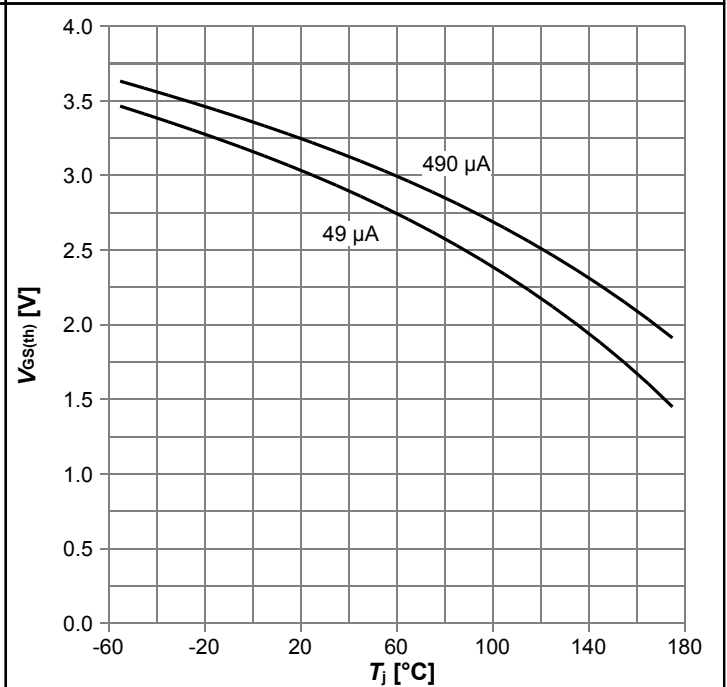
$g_{fs}=f(I_D)$; $T_j=25\text{ }^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



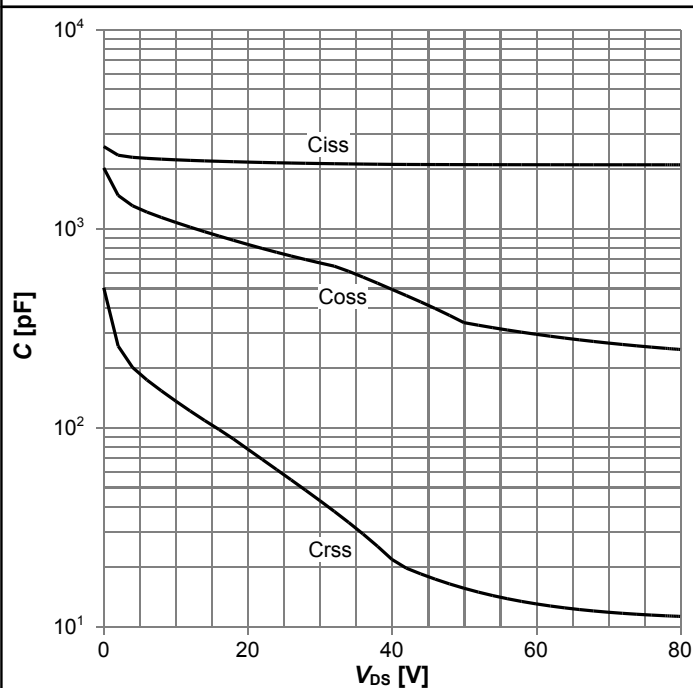
$R_{DS(on)}=f(T_j)$; $I_D=44$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



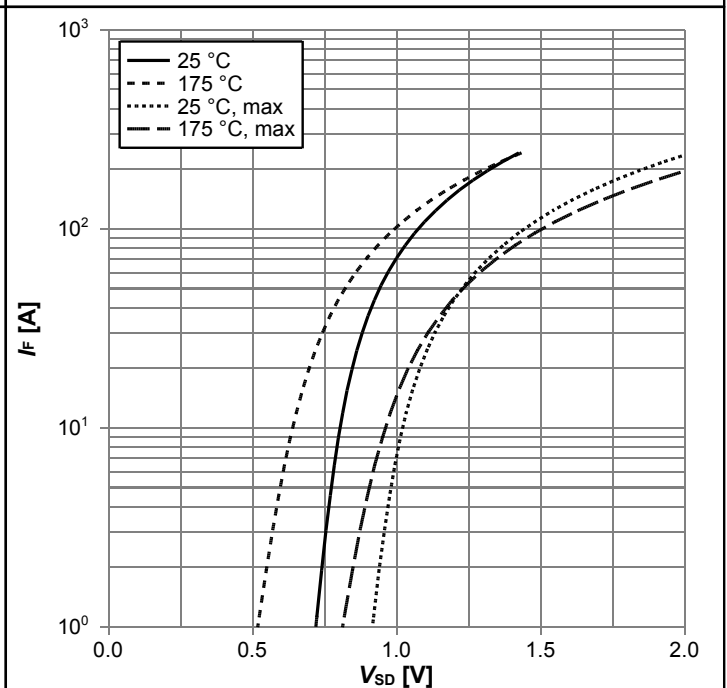
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



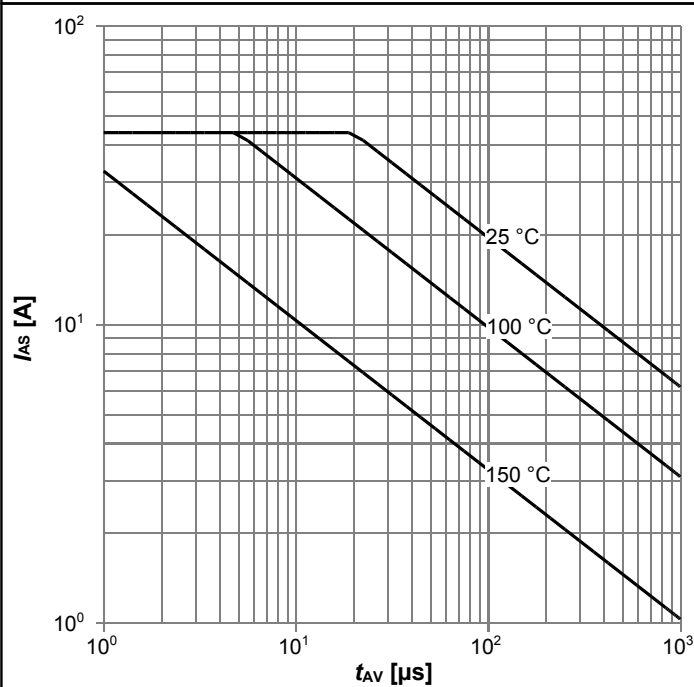
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



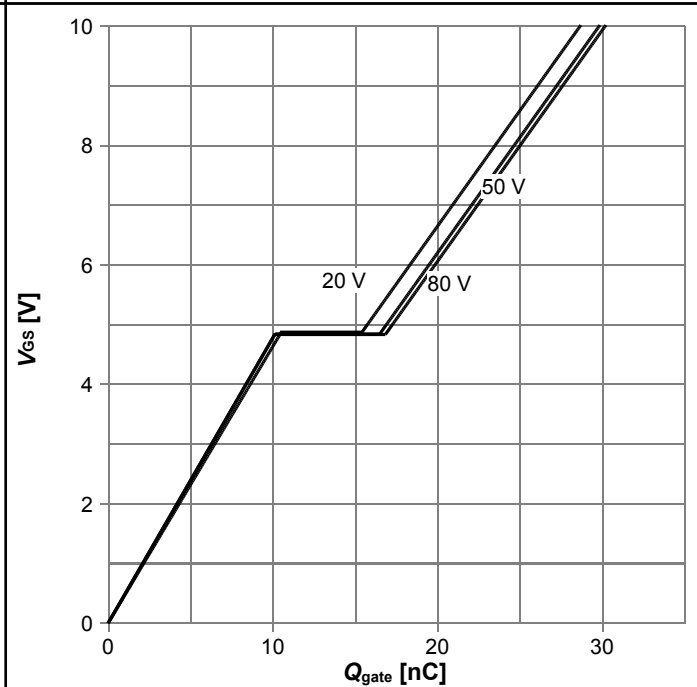
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



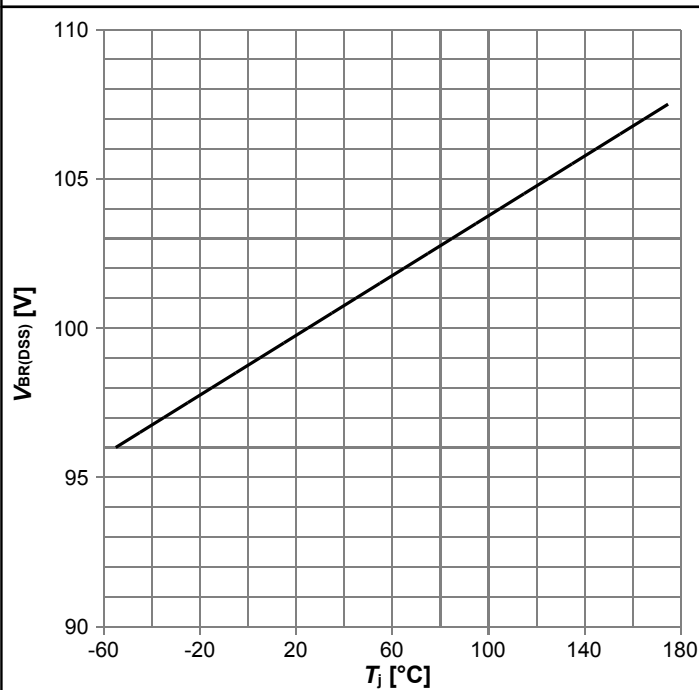
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



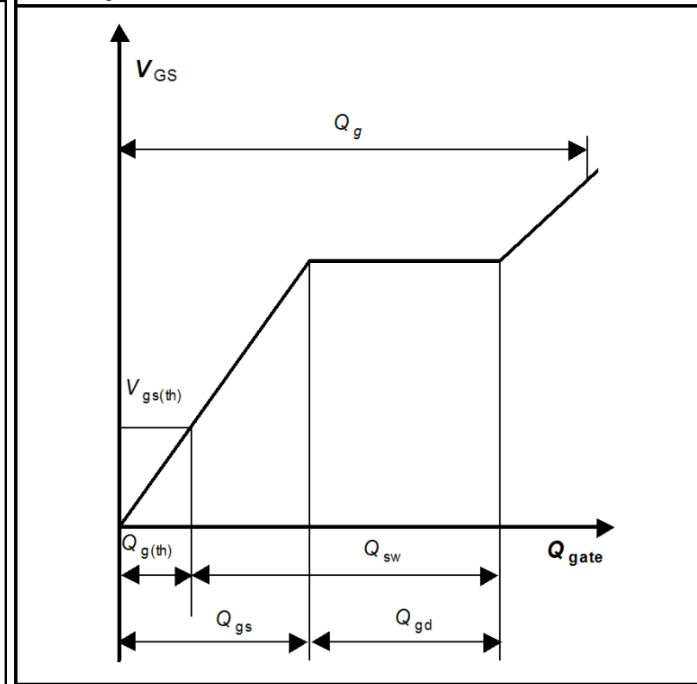
$V_{GS}=f(Q_{gate}); I_D=44 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

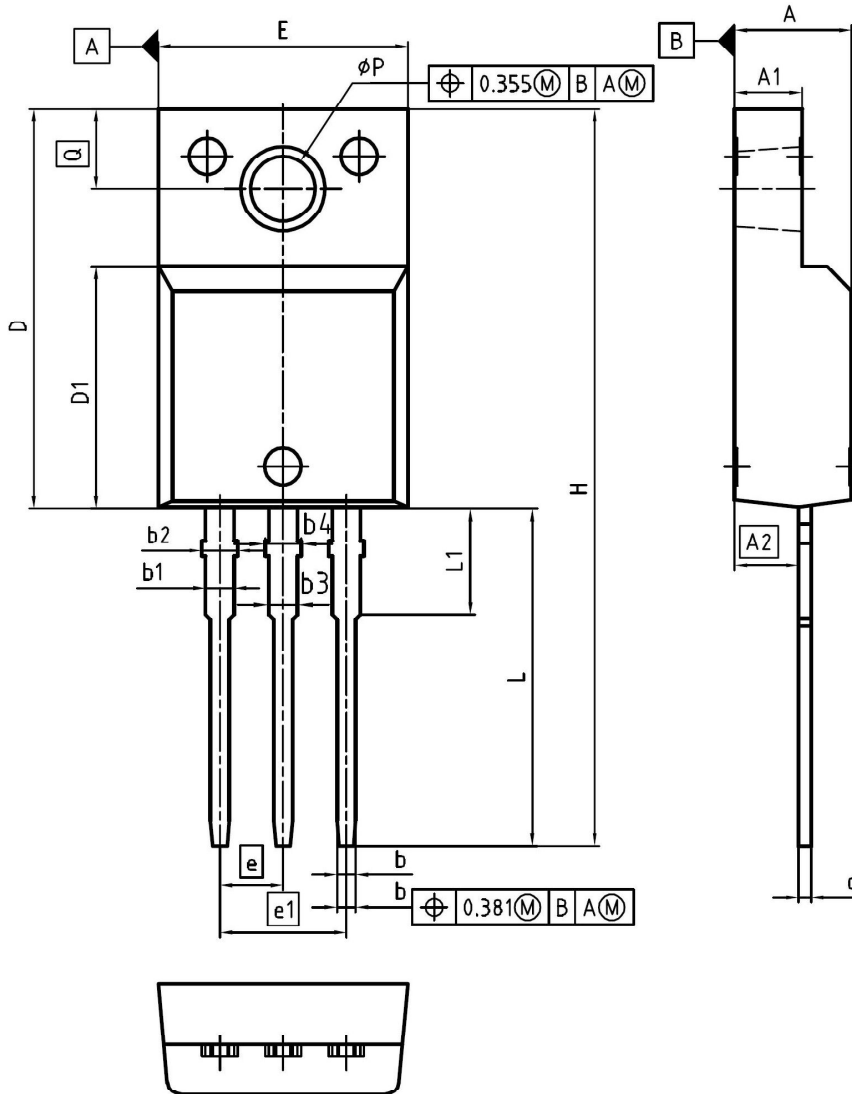


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.55	4.85	0.179	0.191
A1	2.55	2.85	0.100	0.112
A2	2.42	2.72	0.095	0.107
b	0.65	0.85	0.026	0.033
b1	0.95	1.33	0.037	0.052
b2	0.95	1.51	0.037	0.059
b3	0.65	1.33	0.026	0.052
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.85	16.15	0.624	0.636
D1	9.53	9.83	0.375	0.387
E	10.35	10.65	0.407	0.419
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H	29.45	29.75	1.159	1.171
L	13.45	13.75	0.530	0.541
L1	3.15	3.45	0.124	0.136
φP	2.95	3.20	0.116	0.126
Q	3.15	3.50	0.124	0.138

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SCALE

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REVISION
03

Figure 1 Outline PG-TO220-FP, dimensions in mm/inches

Revision History

IPA083N10N5

Revision: 2014-12-18, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-18	Release of final version

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