OptiMOS™ Power-MOSFET

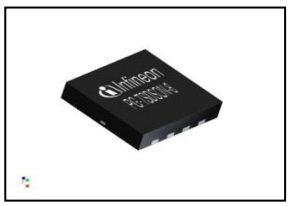
Features

- Optimized for 5V driver application (Notebook, VGA, POL)
- Low FOM_{SW} for High Frequency SMPS
- 100% avalanche tested
- Improved switching behaviour
- N-channel
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Qualified according to JEDEC[1] for target applications
- Superior thermal resistance
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}		34	V
$R_{DS(on),max}$	V_{GS}=10 V	12	mΩ
	V_{GS}=4.5 V	15	
I_D		36	A

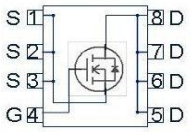
PG-TSDSON-8



RoHS

Halogen-Free

Type	Package	Marking
BSZ0909NS	PG-TSDSON-8	0909NS



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	36	A
		V_{GS}=10 V, T_C=100 °C	23	
		V_{GS}=4.5 V, T_C=25 °C	32	
		V_{GS}=4.5 V, T_C=100 °C	21	
		V_{GS}=4.5 V, T_A=25 °C, R_{thJA}=60 K/W[2]	9	
Pulsed drain current[3]	$I_{D,pulse}$	T_C=25 °C	144	
Avalanche current, single pulse[4]	I_{AS}	T_C=25 °C	20	
Avalanche energy, single pulse	E_{AS}	I_D=20 A, R_{GS}=25 Ω	9	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	25	W
		T_A=25 °C, R_{thJA}=60 K/W[2)]	2.1	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	5.1	K/W
Device on PCB	R_{thJA}	6 cm^2 cooling area[2)]	-	-	60	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	34	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=34 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=34 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=12 A	-	12.0	15	mΩ
		V_{GS}=10 V, I_D=20 A	-	10.0	12.0	
Gate resistance	R_G		1.5	3.0	6.0	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A	24	47	-	S

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3)] See figure 3 for more detailed information

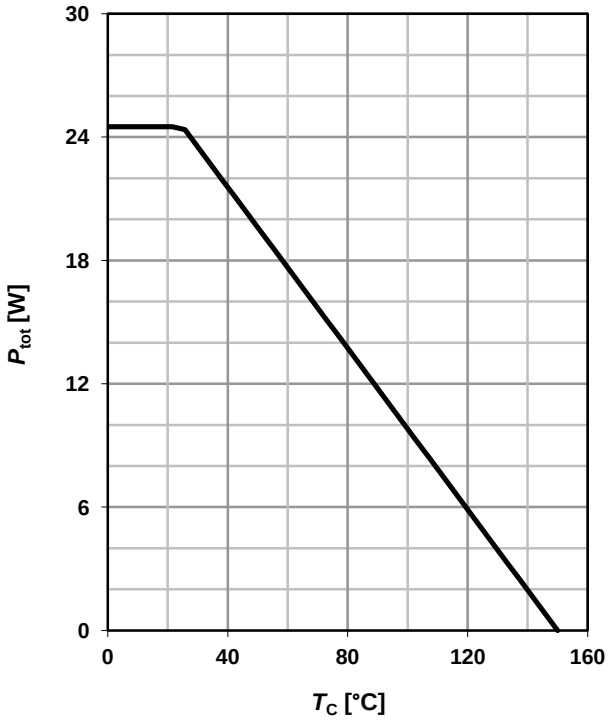
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	975	1310	pF
Output capacitance	C_{oss}		-	340	450	
Reverse transfer capacitance	C_{rss}		-	21	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω	-	4.5	-	ns
Rise time	t_r		-	2.2	-	
Turn-off delay time	$t_{d(off)}$		-	16	-	
Fall time	t_f		-	2.0	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	3.3	4.4	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.5	-	
Gate to drain charge	Q_{gd}		-	1.6	2.1	
Switching charge	Q_{sw}		-	3.2	-	
Gate charge total	Q_g		-	6.1	8.1	
Gate plateau voltage	$V_{plateau}$		-	3.4	-	V
Gate charge total	Q_g	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V	-	13	17	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	5.3	-	
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	8.9	12	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	23	A
Diode pulse current	$I_{S,pulse}$		-	-	148	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=20 A, T_j=25 °C	-	0.9	-	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt =400 A/µs	-	-	10	nC

[4)] See figure 13 for more detailed information

[5)] See figure 16 for gate charge parameter definition

1 Power dissipation

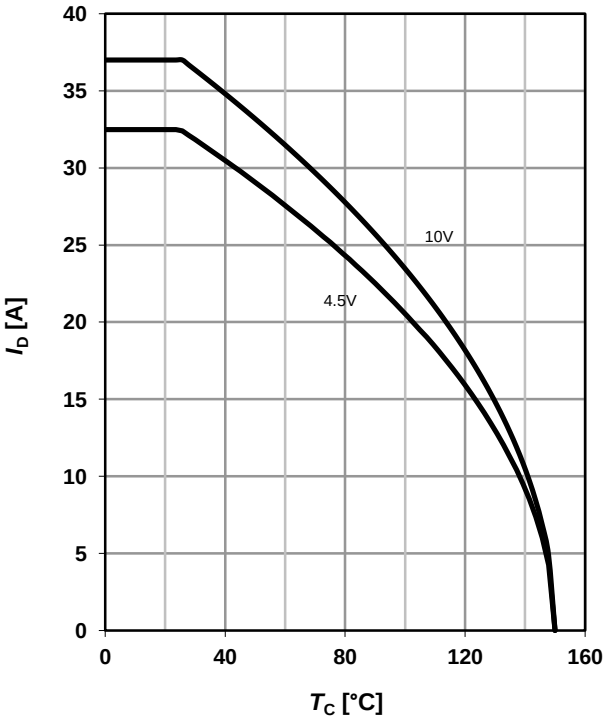
$P_{tot}=f(T_C)$



2 Drain current

$I_D=f(T_C)$

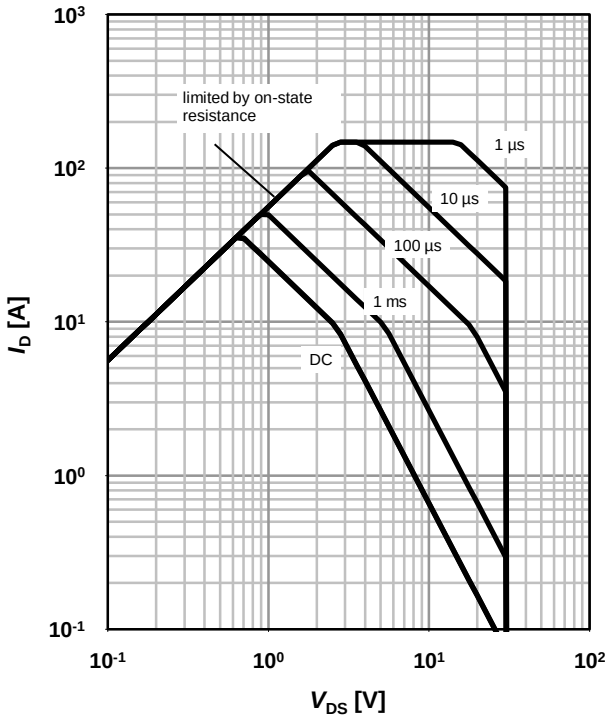
parameter: V_{GS}



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

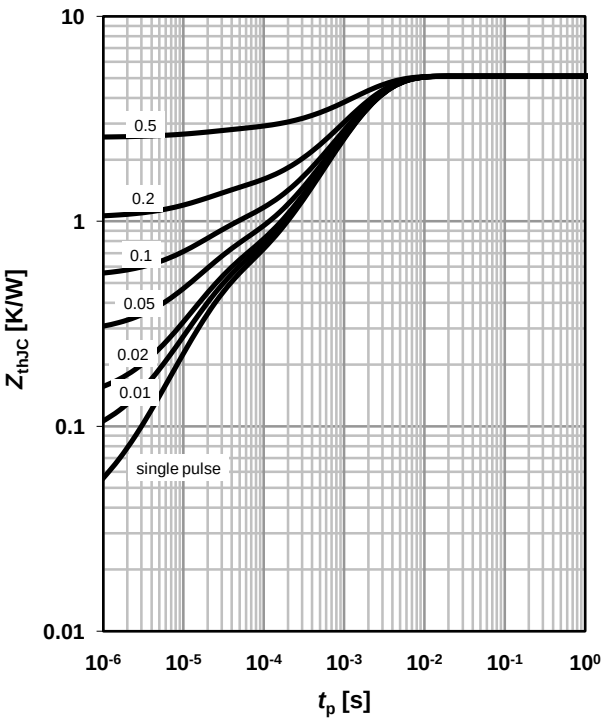
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

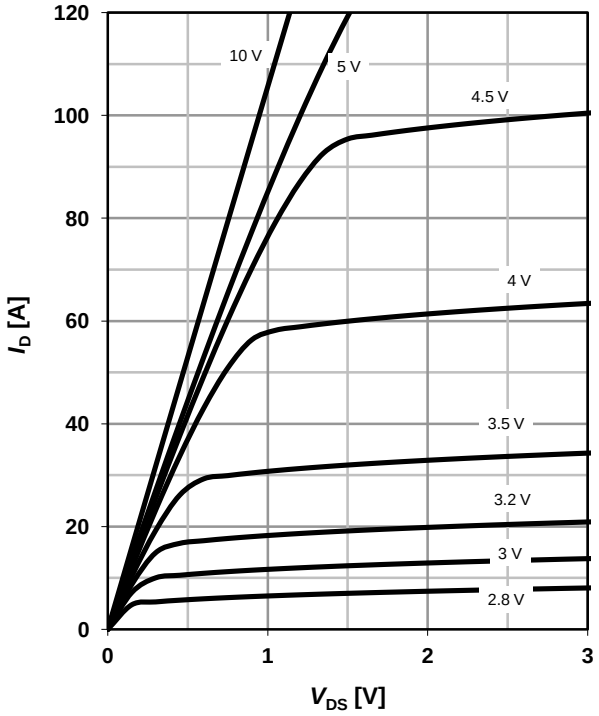
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

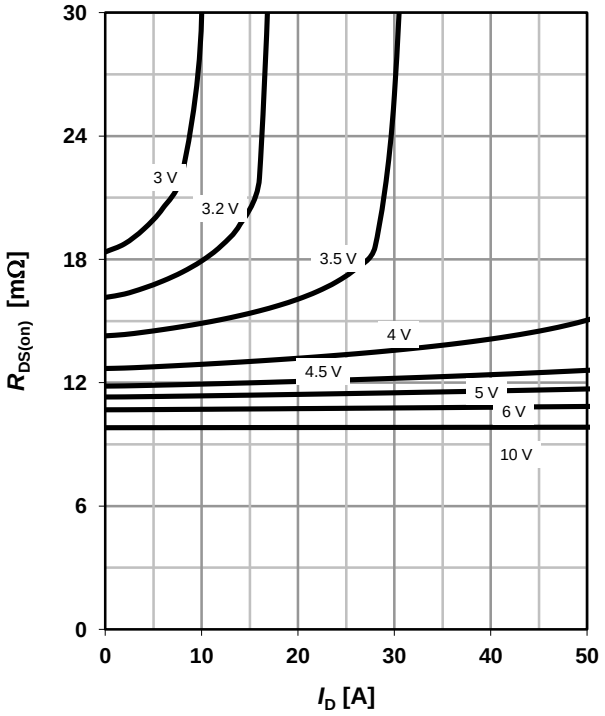
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

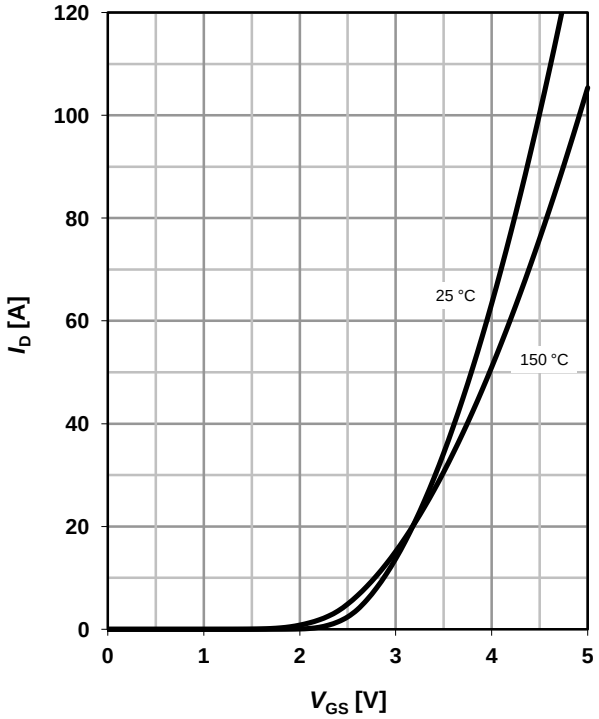
parameter: V_{GS}



7 Typ. transfer characteristics

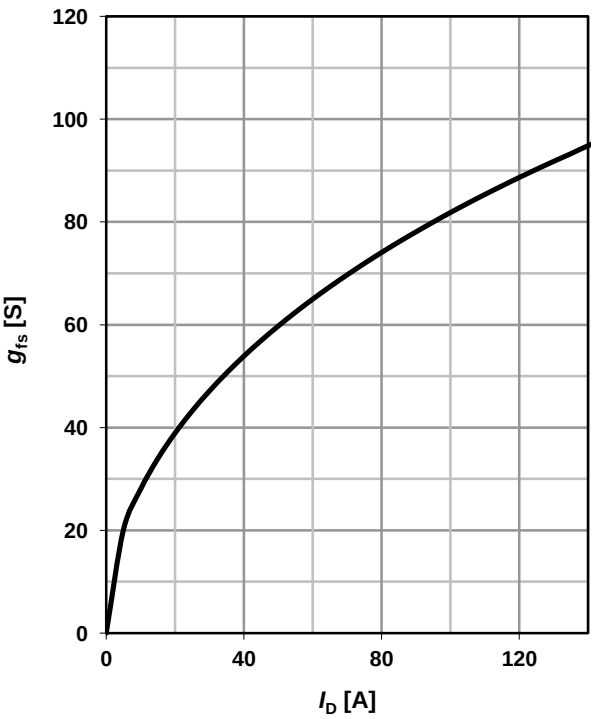
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



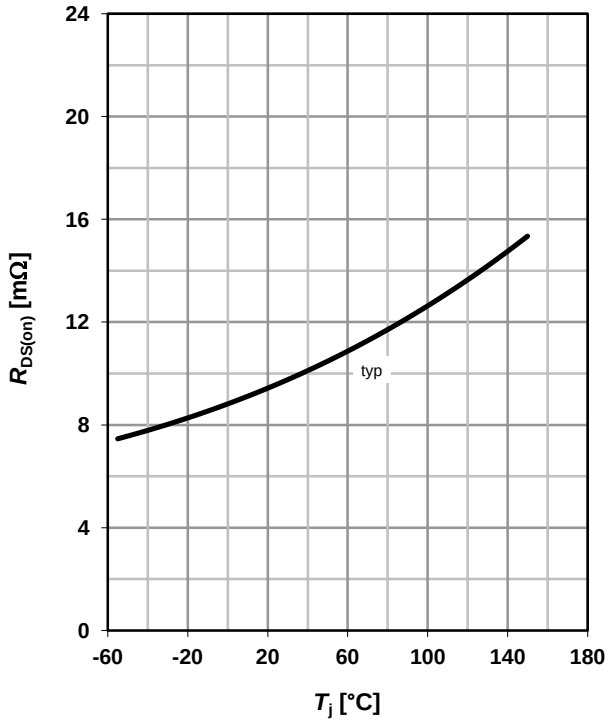
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



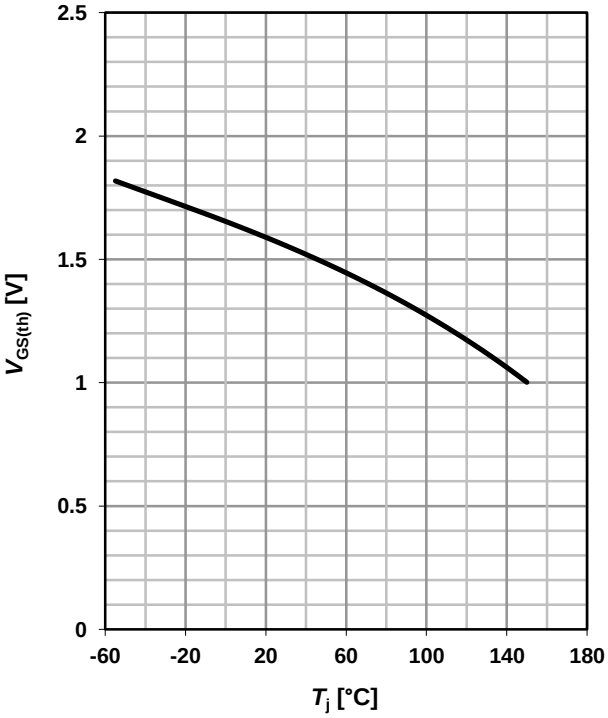
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j)$; $I_D=20$ A; $V_{GS}=10$ V



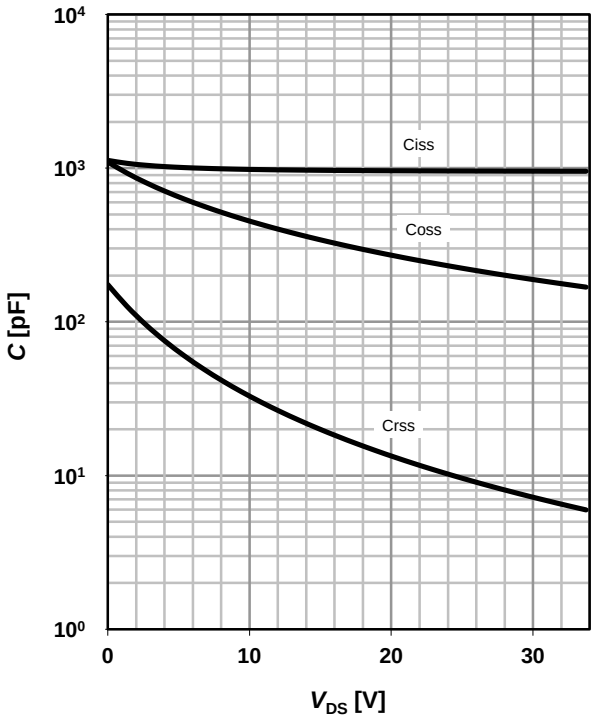
10 Typ. gate threshold voltage

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_D=250$ µA



11 Typ. capacitances

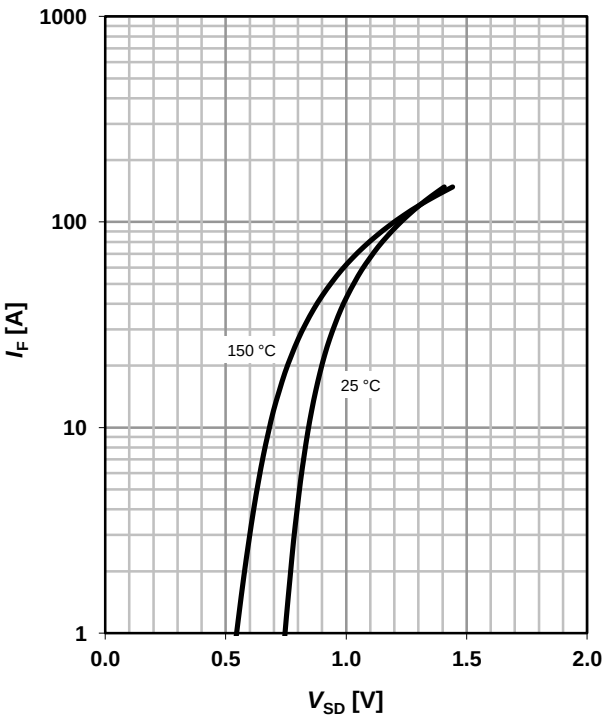
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

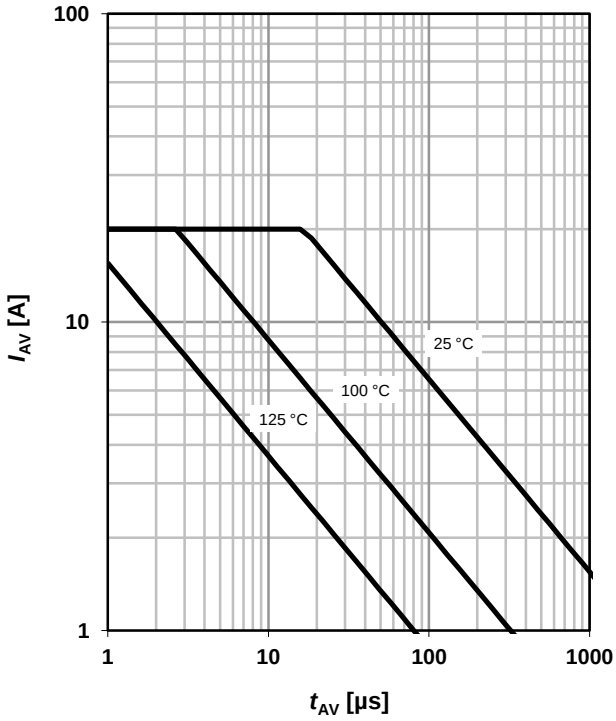
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

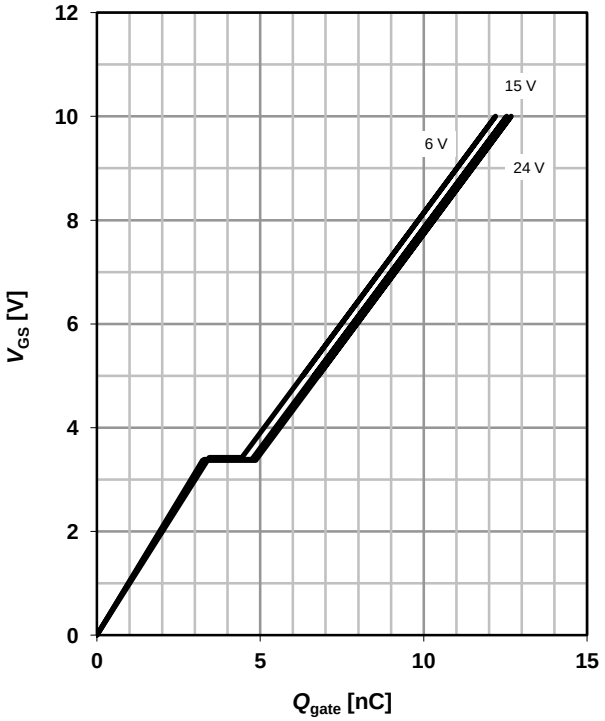
parameter: $T_{j(start)}$



14 Typ. gate charge

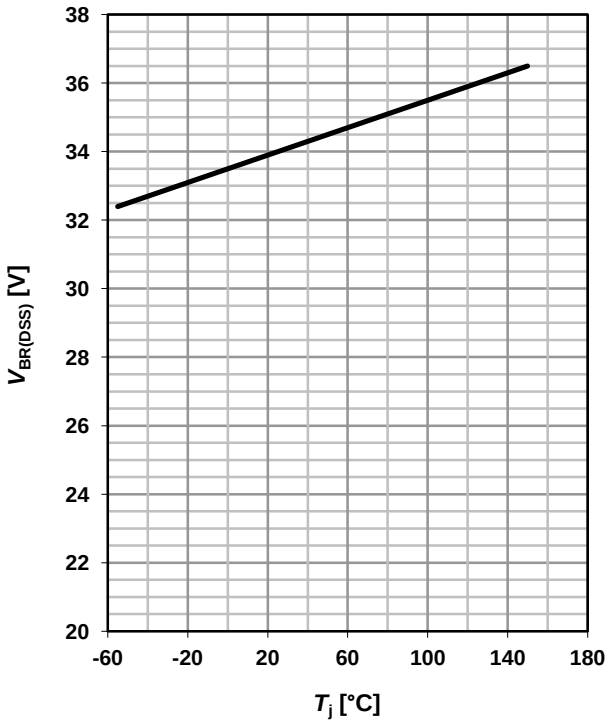
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

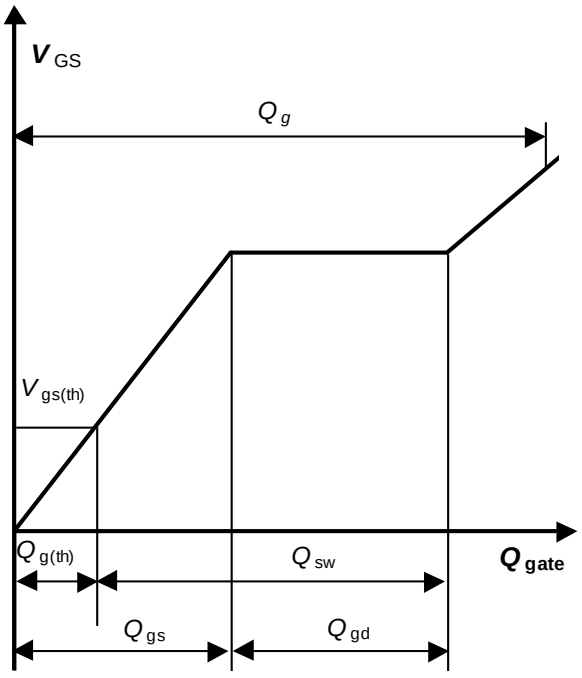


15 Drain-source breakdown voltage

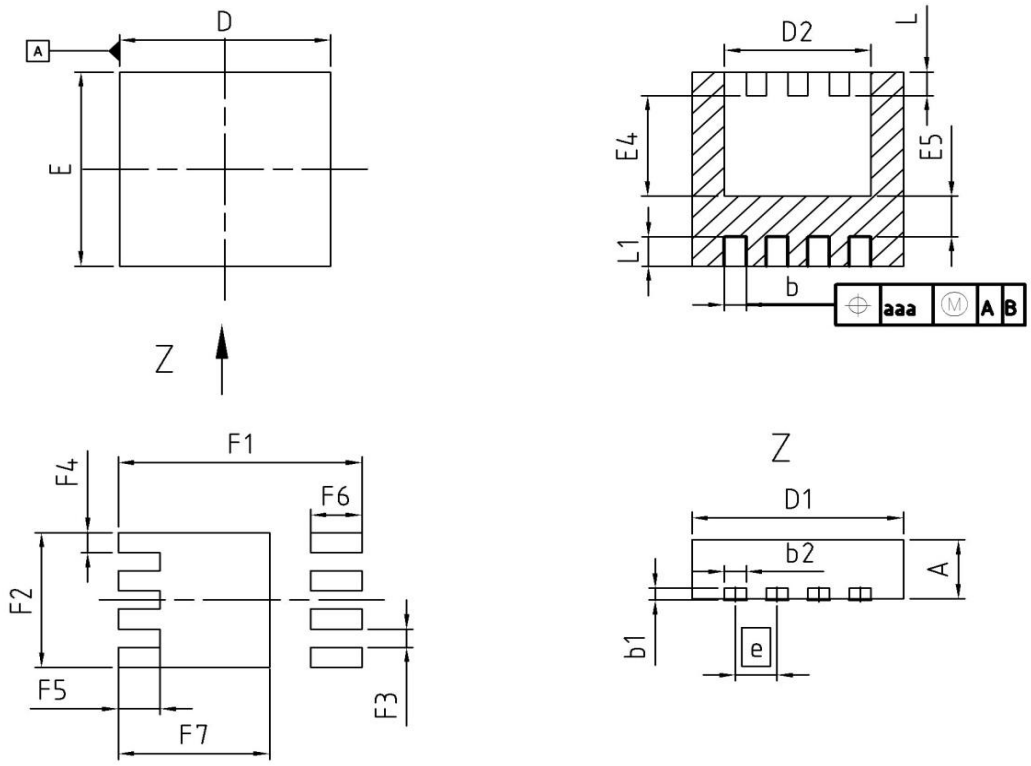
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



Package Outline **PG-TSDSON-8**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.20	0.44	0.008	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.15	2.45	0.085	0.096
E	3.20	3.40	0.126	0.134
E4	1.60	1.81	0.063	0.071
E5	0.59	0.86	0.023	0.034
e	0.65		0.026	
N	8		8	
L	0.30	0.56	0.012	0.022
L1	0.33	0.60	0.013	0.024
aaa	0.25		0.010	
F1	3.80		0.150	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.65		0.026	
F6	0.80		0.031	
F7	2.36		0.093	

DOCUMENT NO.
Z8B00131645

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
17-09-2008

REVISION
02

Published by
Infineon Technologies AG
81726 Munich, Germany

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