

**OptiMOS™ Power-MOSFET**
**Features**

- Optimized for synchronous rectification
- Integrated monolithic Schottky-like diode
- Very low on-resistance  $R_{DS(on)}$
- 100% avalanche tested
- N-channel, logic level
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability due to enlarged source interconnection



Type	Package	Marking
BSC010N04LSI	PG-TDSON-8 FL	010N04LI

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	100	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	100	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	100	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	100	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$	37	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	400	
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	$T_C=25\text{ °C}$	50	
Avalanche energy, single pulse	$E_{AS}$	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$	230	mJ
Gate source voltage	$V_{GS}$		$\pm 20$	V

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See figure 3 for more detailed information

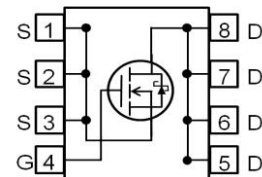
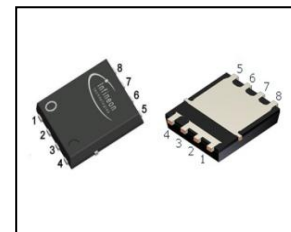
<sup>4)</sup> See figure 13 for more detailed information

**Product Summary**

$V_{DS}$	40	V
$R_{DS(on),max}$	1.05	m $\Omega$
$I_D$	100	A
$Q_{OSS}$	83	nC
$Q_G(0V..10V)$	87	nC

**PG-TDSON-8 FL**

enlarged source interconnection



**Maximum ratings**, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	139	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=50\text{ K/W}^2$	2.5	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{\text{thJC}}$	bottom	-	-	0.9	K/W
		top	-	-	20	
Device on PCB	$R_{\text{thJA}}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	50	

**Electrical characteristics**, at  $T_j=25\text{ °C}$ , unless otherwise specified

**Static characteristics**

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$ , $I_{\text{D}}=10\text{ mA}$	40	-	-	V
Breakdown voltage temperature coefficient	$\frac{dV_{(\text{BR})\text{DSS}}}{dT_j}$	$I_{\text{D}}=10\text{ mA}$ , referenced to 25 °C	-	30	-	mV/K
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$ , $I_{\text{D}}=250\text{ }\mu\text{A}$	1.2	-	2	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=32\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=25\text{ °C}$	-	-	0.5	mA
		$V_{\text{DS}}=32\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=125\text{ °C}$	-	3	-	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}$ , $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}$ , $I_{\text{D}}=50\text{ A}$	-	1.1	1.4	mΩ
		$V_{\text{GS}}=10\text{ V}$ , $I_{\text{D}}=50\text{ A}$	-	0.9	1.05	
Gate resistance	$R_{\text{G}}$		-	0.8	-	Ω
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$ , $I_{\text{D}}=50\text{ A}$	130	260	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$	-	6200	-	pF
Output capacitance	$C_{oss}$		-	1900	-	
Reverse transfer capacitance	$C_{rss}$		-	140	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A}, R_{G,ext}=1.6\ \Omega$	-	22	-	ns
Rise time	$t_r$		-	48	-	
Turn-off delay time	$t_{d(off)}$		-	72	-	
Fall time	$t_f$		-	17	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	15	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	9.9	-	
Gate to drain charge	$Q_{gd}$		-	14	-	
Switching charge	$Q_{sw}$		-	19	-	
Gate charge total	$Q_g$		-	87	-	
Gate plateau voltage	$V_{plateau}$		-	2.4	-	
Gate charge total	$Q_g$	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }4.5\text{ V}$	-	45	-	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }10\text{ V}$	-	76	-	
Output charge	$Q_{oss}$	$V_{DD}=20\text{ V}, V_{GS}=0\text{ V}$	-	83	-	

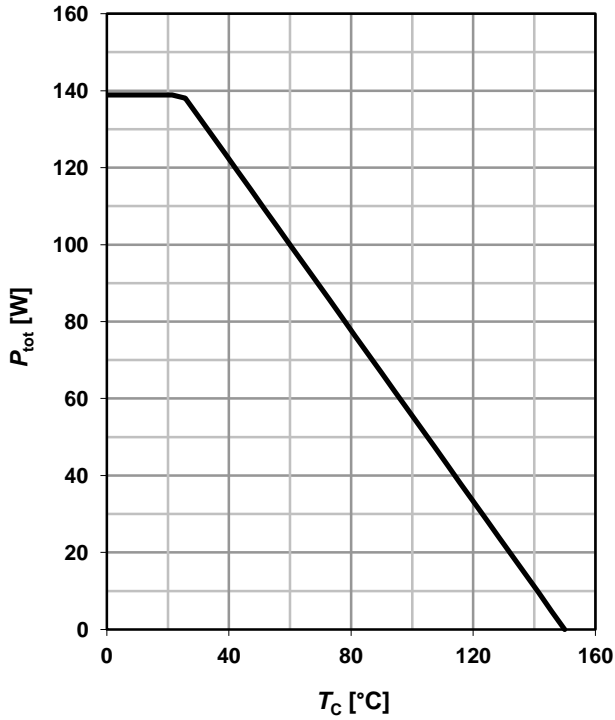
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	100	A
Diode pulse current	$I_{S,pulse}$		-	-	400	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=20\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.57	0.7	V
Reverse recovery charge	$Q_{rr}$	$V_R=20\text{ V}, I_F=20\text{ A}, di_F/dt=400\text{ A}/\mu\text{s}$	-	20	-	nC

<sup>5)</sup> See figure 16 for gate charge parameter definition

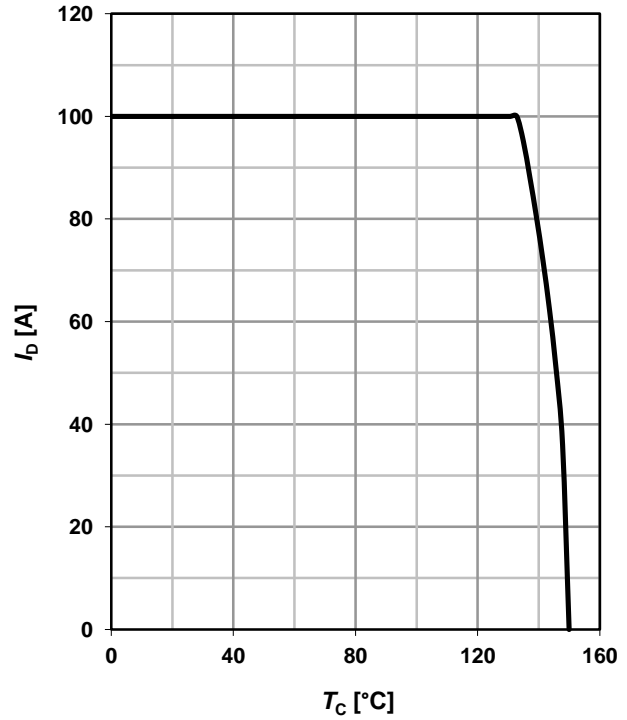
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

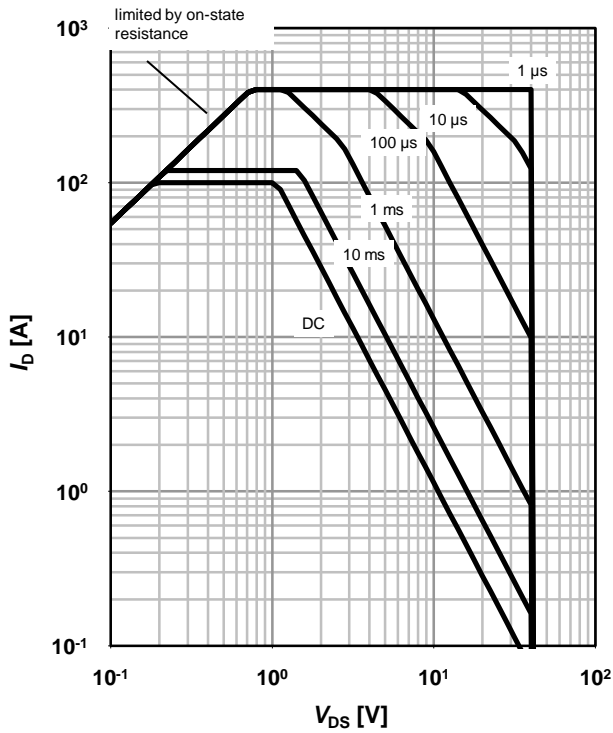
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



**3 Safe operating area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

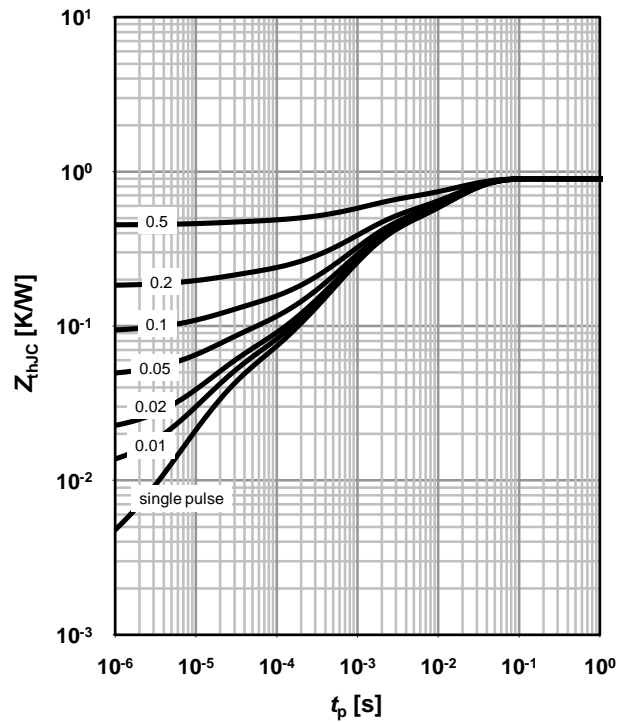
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

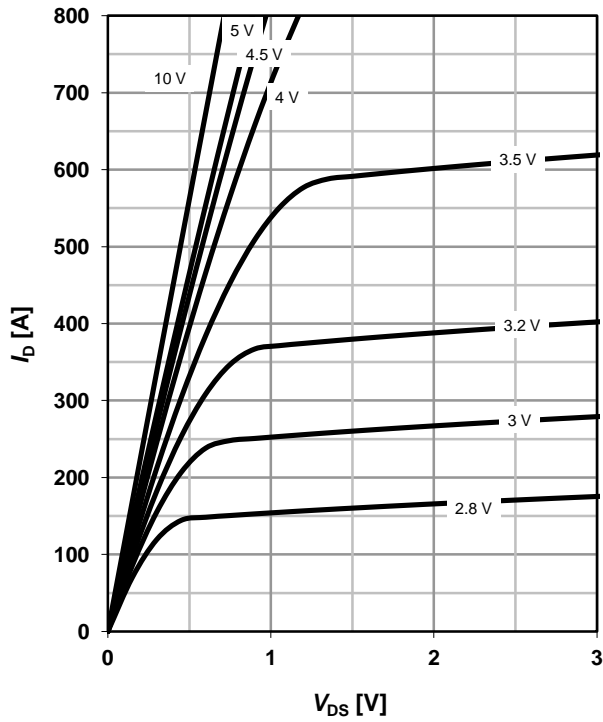
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

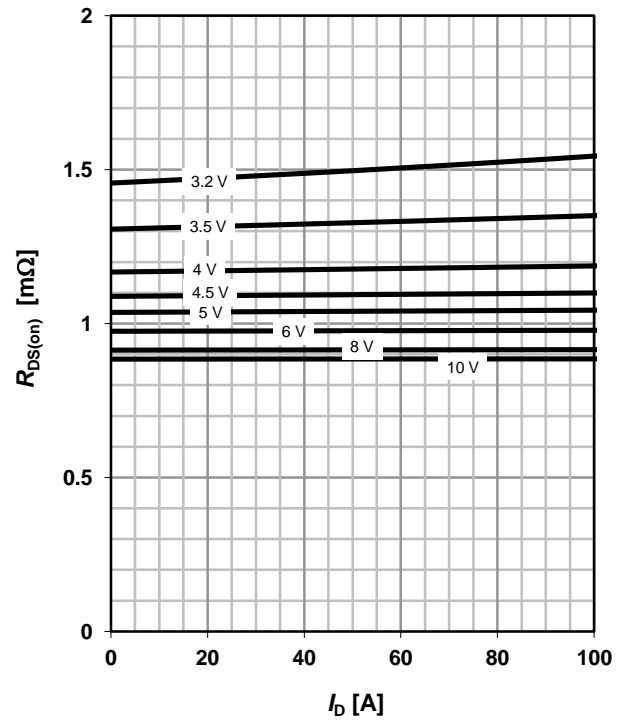
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

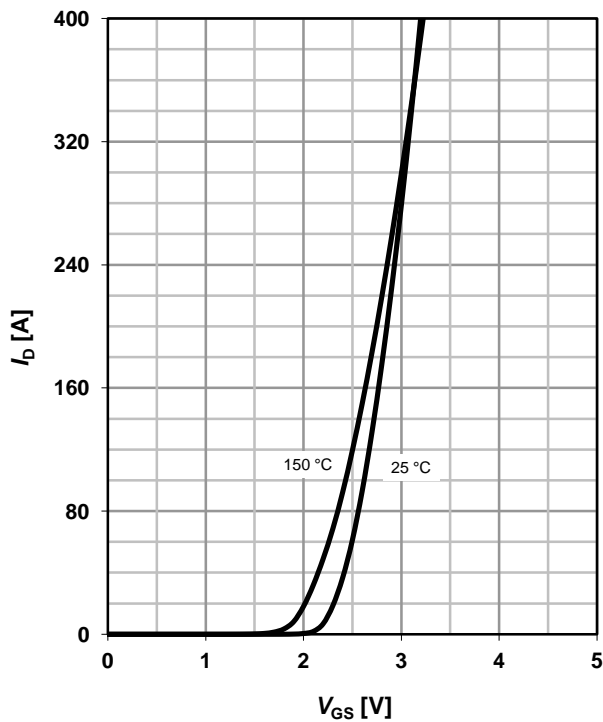
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

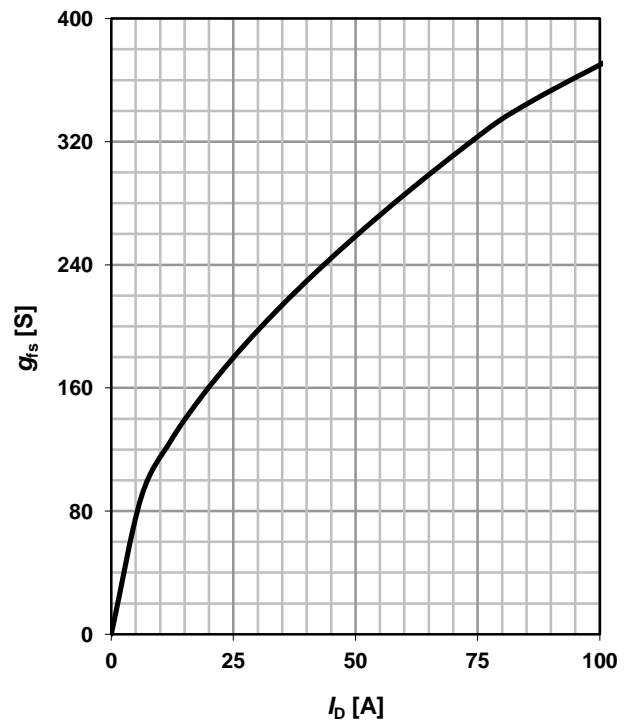
$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}$

parameter:  $T_j$



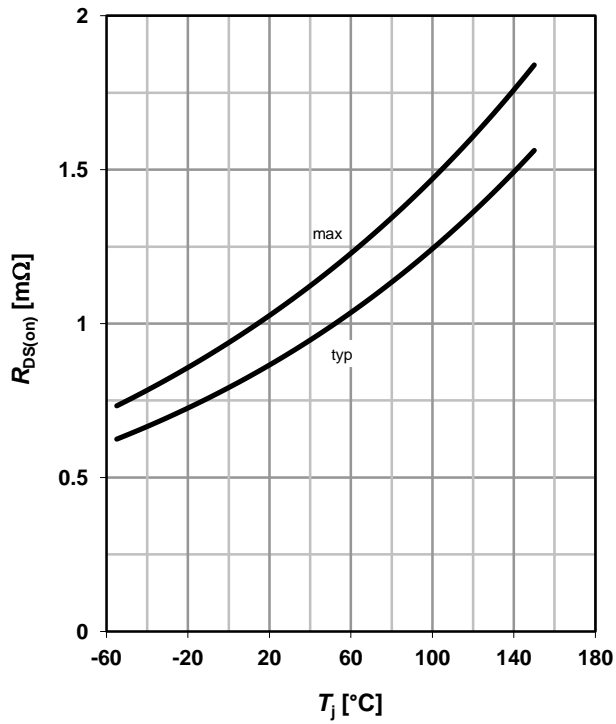
**8 Typ. forward transconductance**

$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$



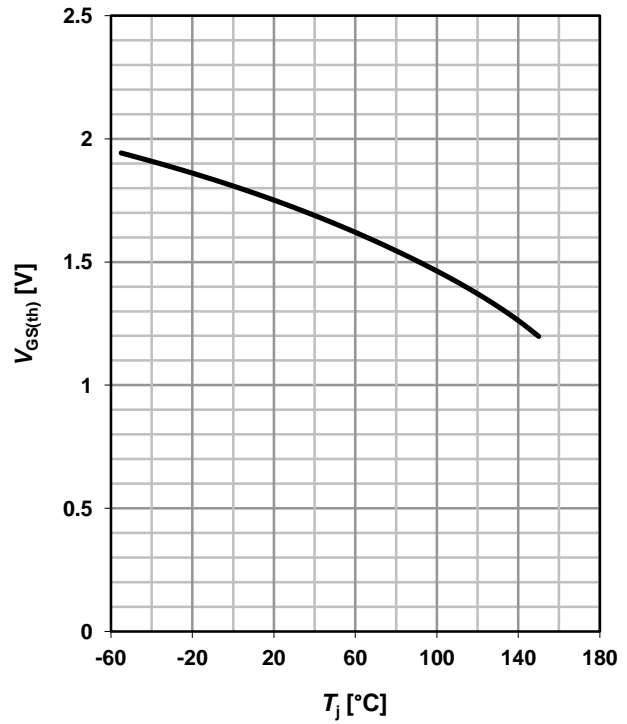
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=50\text{ A}; V_{GS}=10\text{ V}$



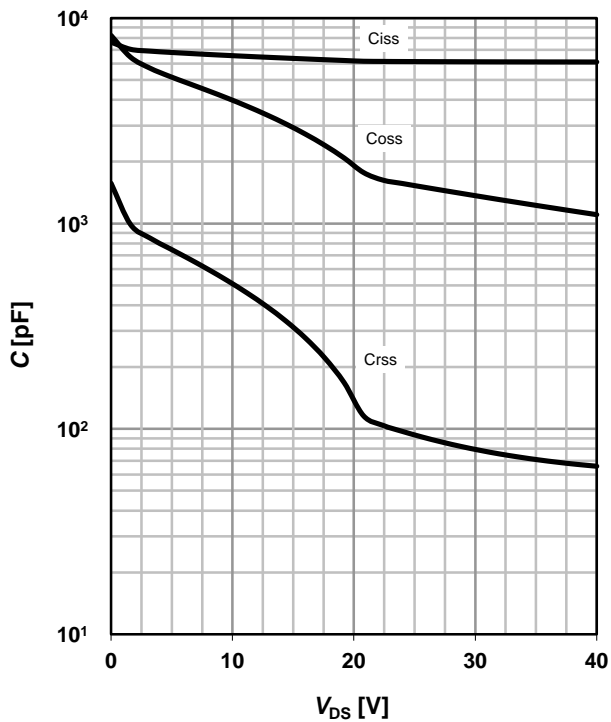
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_{DS}=10\text{ mA}$



**11 Typ. capacitances**

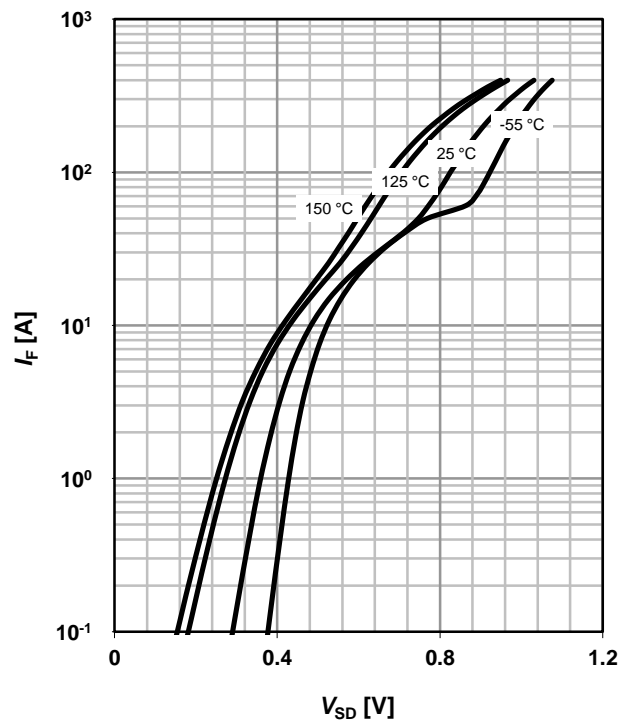
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

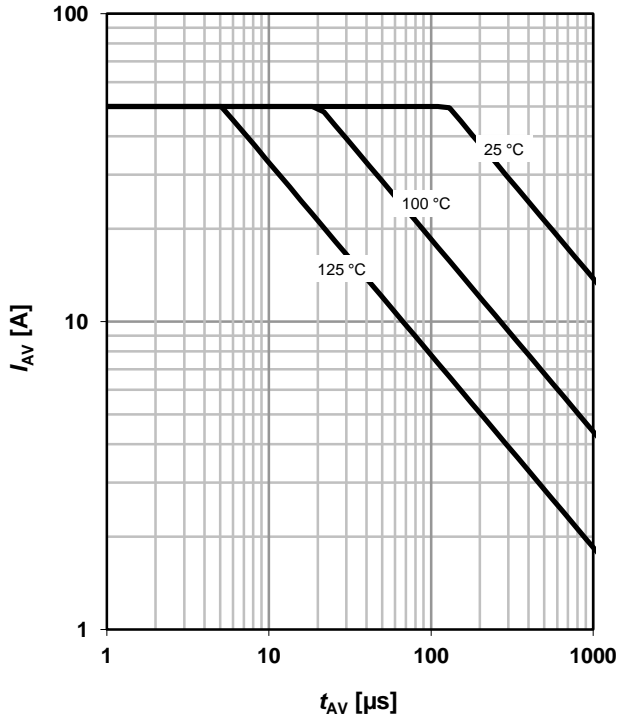
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

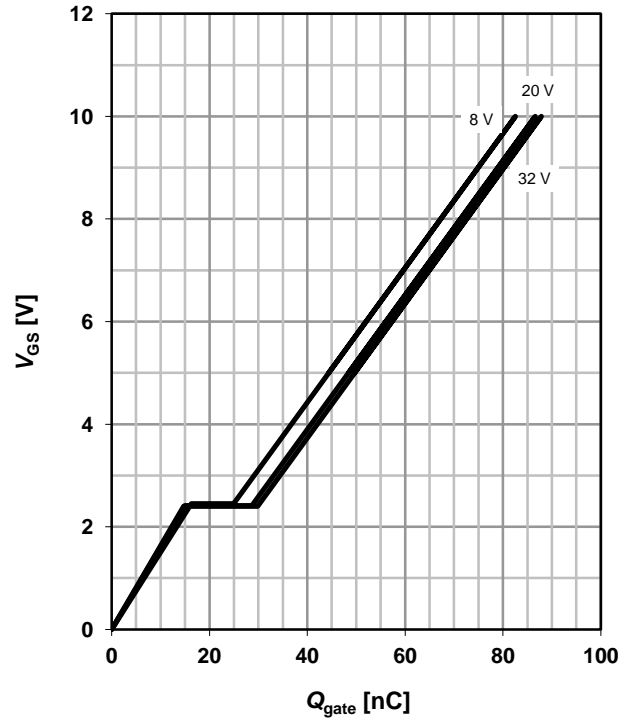
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

$V_{GS}=f(Q_{gate}); I_D=50 \text{ A pulsed}$

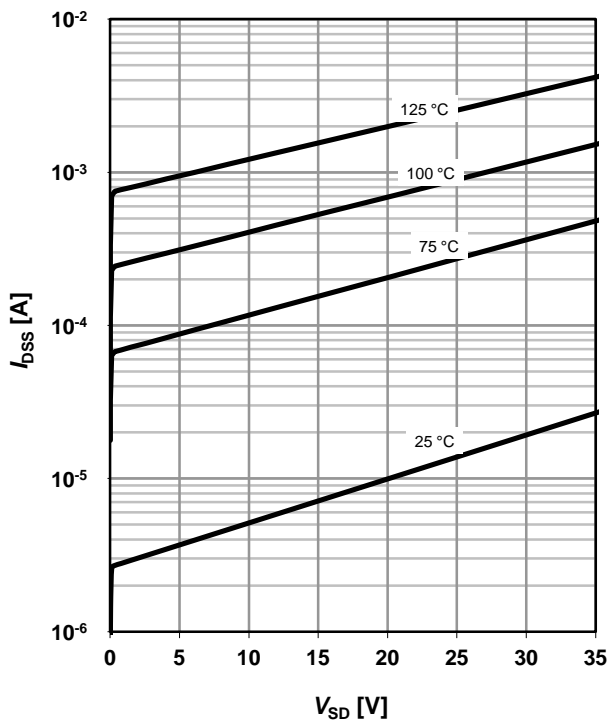
parameter:  $V_{DD}$



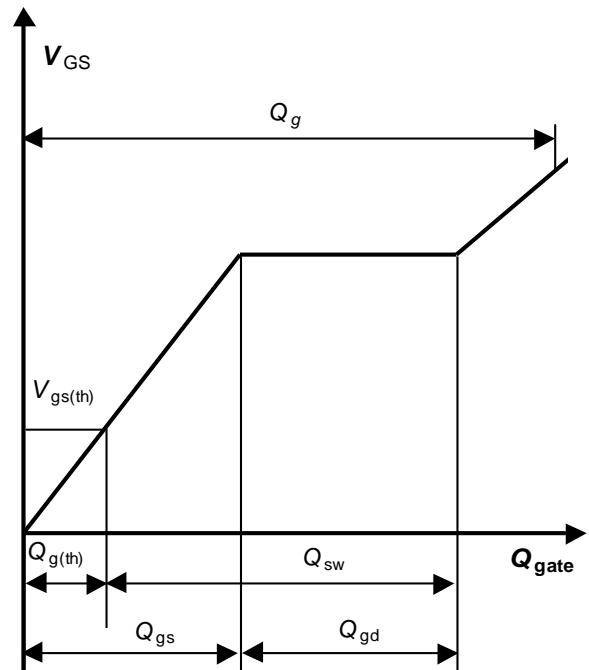
**15 Typ. drain-source leakage current**

$I_{DSS}=f(V_{DS}); V_{GS}=0 \text{ V}$

parameter:  $T_j$



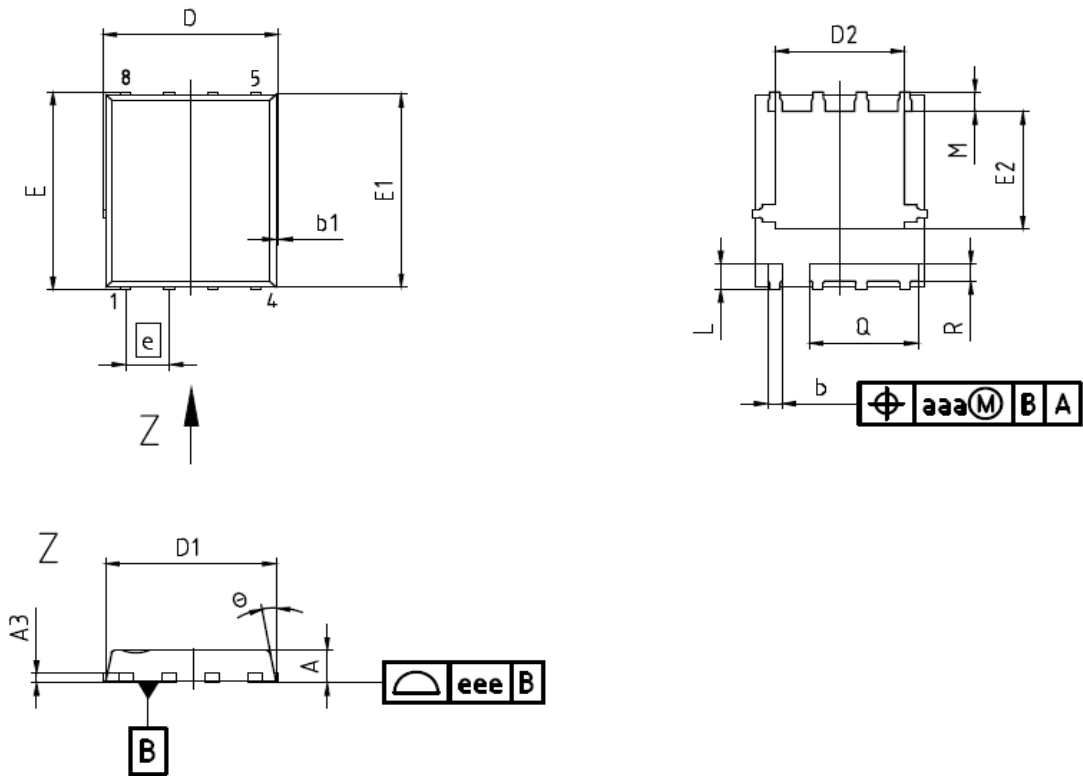
**16 Gate charge waveforms**



Package Outline

PG-TDSON-8 FL

PG-TDSON-8 FL: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
A3	0.25 (REF)		0.011 (REF)	
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.009
D	5.15 (BSC)		0.203 (BSC)	
D1	5.00 (BSC)		0.197 (BSC)	
D2	3.70	4.40	0.146	0.173
E	6.15 (BSC)		0.242 (BSC)	
E1	6.00 (BSC)		0.236 (BSC)	
E2	3.40	3.80	0.134	0.150
e	1.27 (BSC)		0.050 (BSC)	
N	8		8	
L	0.74	0.84	0.029	0.033
M	0.45	0.66	0.018	0.026
theta	8.5°	12°	8.5°	12°
Q	3.15	3.25	0.124	0.128
R	0.48	0.58	0.019	0.023
aaa	0.25		0.010	
eee	0.08		0.003	

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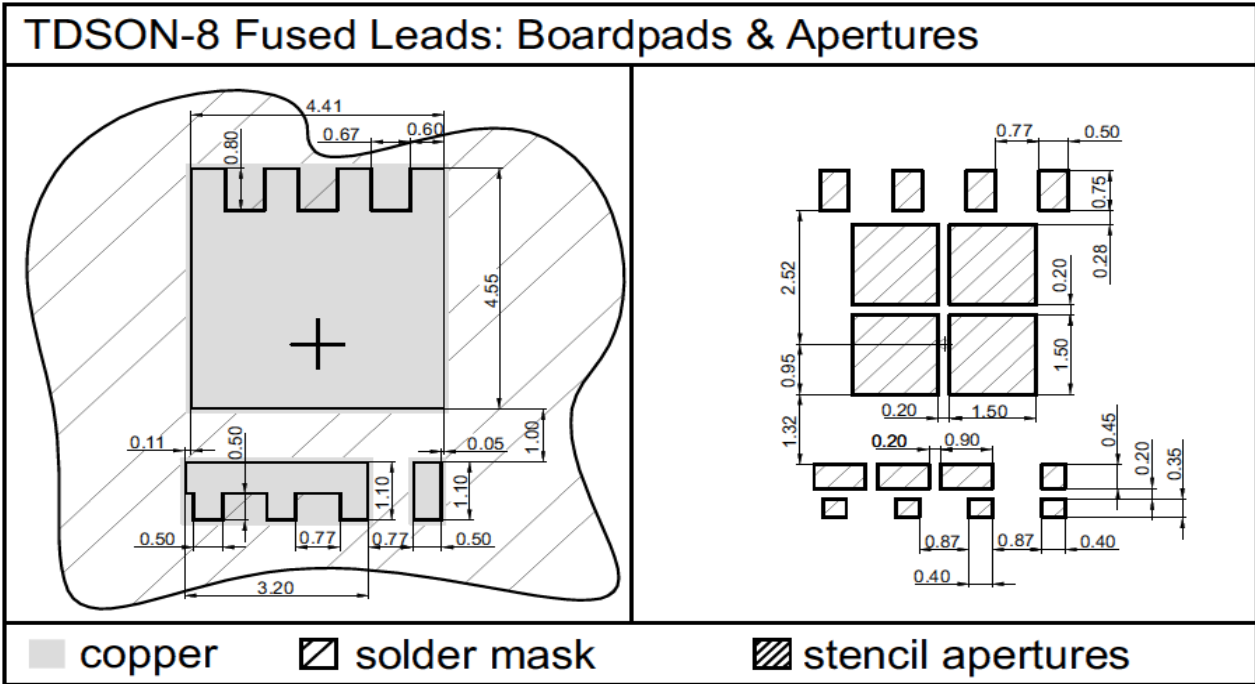
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Package Outline

PG-TDSON-8 FL

PG-TDSON-8 FL: Footprint





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