AOZ5049QI

High-Current, High-Performance DrMOS Power Module

General Description

The AOZ5049QI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High Side (HS) MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low Side (LS) MOSFET has ultra low on-resistance to minimize conduction loss. The compact 3.5mm x 5mm QFN package is optimally chosen and designed to minimize parasitic inductance for minimal EMI signature.

The AOZ5049QI is intended for use with TTL and tri-state compatibility by using both the PWM and /or FCCM inputs for accurate control of the power MOSFETs.

A number of features provided make the AOZ5049QI a highly versatile power module. The bootstrap supply diode is integrated in the driver. The LS MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The pinout is optimized for low inductance routing of the converter, keeping the parasitics and their effects to a minimum.

Features

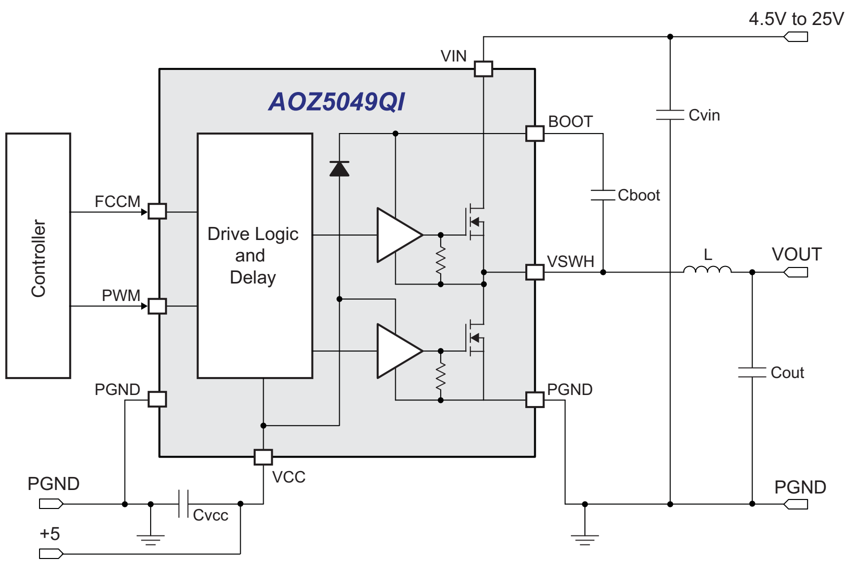
- 4.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- Up to 35A output current
- Integrated bootstrap Schottky diode
- Up to 2MHz switching operation
- Tri-state FCCM/PWM input compatible
- Under-voltage lockout protection
- Single pin control for shutdown/diode emulation/CCM operation
- Small 3.5mm x 5mm QFN-24L package

Applications

- Servers
- Notebook computers
- VRMs for motherboards
- Point-of-load DC/DC converters
- Memory and graphic cards
- Video gaming consoles

Green Product

Typical Application Circuit

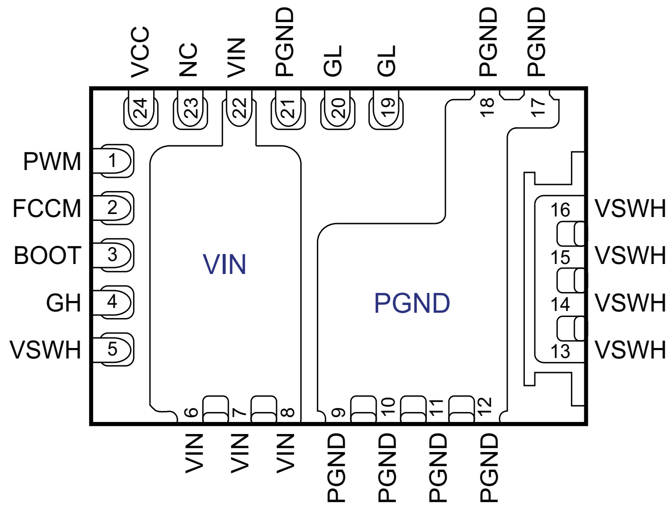


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5049QI	-40°C to +85°C	3.5mm x 5mm QFN-24L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

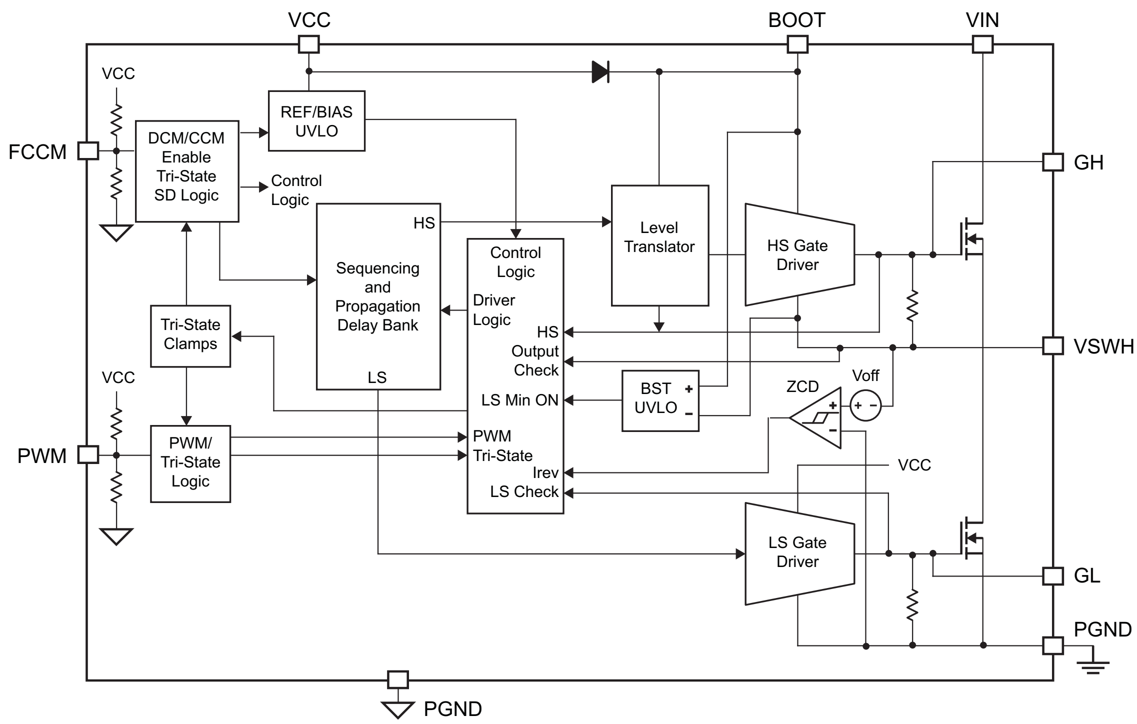


3.5mm x 5mm QFN-24
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. This input is compatible with 5V and Tri-State logic level Low Side.
2	FCCM	Continuous conduction mode of operation is allowed when FCCM = High. Discontinuous mode is allowed and diode emulation mode is active when FCCM = Low. High impedance on the input of FCCM will shutdown both HS and LS MOSFETs.
3	BOOT	HS MOSFET Gate Driver supply rail (5V wrt VSWH). Connect a 100nF ceramic capacitor between BOOT and the VSWH (Pin 5).
4	GH	HS MOSFET Gate pin.
5	VSWH	Switching node connected to the source of HS MOSFET and the drain of LS MOSFET. This pin is dedicated for bootstrap capacitor connection to the BOOT pin. It is optional to connect to Pin 13 externally on PCB.
6, 7, 8	VIN	Power stage high voltage input pin.
9, 10, 11, 12, 17, 18	PGND	Power Ground pin for power stage.
13, 14, 15, 16	VSWH	Switching node connected to the source of HS MOSFET and the drain of LS MOSFET. These pins are being used for Zero Cross Detect, Bootstrap UVLO and Anti-Overlap Control.
19, 20	GL	LS MOSFET Gate pin.
21	PGND	Power Ground pin for LS MOSFET Gate Driver.
22	VIN	Power stage high voltage input pin.
23	NC	No Connect. Optional connection to Pin 24 rendering no effect in performance and operation.
24	VCC	Serves as Input Bias and LS MOSFET Gate Driver Rail. Connect a 2.2µF MLCC directly across to this pin and PGND (Pin 21).

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC)	-0.3V to 7V
High Voltage Supply (VIN)	-0.3V to 30V
Control Inputs (PWM, FCCM)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 33V
Bootstrap Voltage DC (BOOT-VSWH)	-0.3V to 7V
BOOT Voltage Transient [1] (BOOT-VSWH)	-0.3V to 9V
Switch Node Voltage DC (VSWH)	-0.3V to 30V
Switch Node Voltage Transient[1] (VSWH)	-0.3V to 38V
High Side Gate Voltage DC (GH)	(VSWH-0.3V) to BOOT
High Side Gate Voltage Transient[2] (GH)	(VSWH-5V) to BOOT
Low Side Gate Voltage DC (GL)	(PGND-0.3V) to (VCC+0.3V)
Low Side Gate Voltage Transient[2] (GL)	(PGND-2.5V) to (VCC+0.3V)
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	125°C
ESD Rating[3]	2kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	4.5V to 25V
Low Voltage Supply {VCC, (BOOT-VSWH)}	4.5V to 5.5V
Control Inputs (PWM, FCCM)	0V to (VCC-0.3V)
Operating Frequency	200kHz to 2MHz

Electrical Characteristics(4)

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Power Stage Power Supply		4.5		25	V
V_{CC}	Driver Power Supply	VCC = 5V	4.5		5.5	V
$R_{\theta JC}$	Thermal Resistance	PCB Temp = 100°C		3		°C / W
$R_{\theta JA}$		AOS Demo Board		10		°C / W
INPUT SUPPLY AND UVLO						
V_{CC}	Under-Voltage Lockout	VCC Rising		3.4	3.9	V
V_{CC_HYST}		VCC Falling		500		mV
I_{VCC_SD}	Shutdown Bias Supply Current	FCCM = Floating (Shutdown) VPWM = Internally Pulled Low		3		μA
I_{VCC}	Control Circuit Bias Current	FCCM = 5V (CCM), VPWM = Floating		80		μA
		FCCM = 0V (DCM), VPWM = Floating		120		μA
	Switching Current (I_{BIAS} + I_{DRV})	FCCM = 5V, VPWM = 800kHz		27		mA
		FCCM = 5V, VPWM = 1MHz		34		mA
		FCCM = 5V, VPWM = 1.5MHz		48		mA
PWM INPUT						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, VCC = 5V	4.1			V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, VCC = 5V			0.7	V
I_{PWM}	PWM Pin Input Current	Source, PWM = 5V		+250		μA
		Sink, PWM = 0V		-250		μA
V_{TRI}	PWM Input Tri-State Threshold Window	PWM = High Impedance	1.1		3.9	V
FCCM INPUT						
V_{FCCMH}	FCCM Enable Threshold	FCCM Rising, VCC = 5V Shutdown → CCM	3.8			V
V_{FCCML}		FCCM Falling, VCC = 5V Shutdown → DCM			1.2	V
I_{FCCM}	FCCM Pin Input Current	Source, FCCM = 5V		+50		μA
		Sink, FCCM = 0V		-50		μA
V_{TRI}	FCCM Input Tri-State Threshold Window	FCCM = High Impedance	1.4		3.4	V
V_{TRI_HYST}	FCCM Input Threshold Hysteresis	Shutdown → CCM → Shutdown DCM → Shutdown → DCM		300		mV
t_{PTS}	PS4 Exit Latency	VCC = 5V			15	μs
GATE DRIVER TIMING						
t_{PDLU}	PWM Falling to GH Turn-Off	PWM 10%, GH 90%		18		ns
t_{PDLL}	PWM Raising to GL Turn-Off	PWM 90%, GL 90%		25		ns
t_{PDHU}	GL Falling to GH Rising Deadtime	GL 10%, GH 10%		20		ns
t_{PDHL}	GH/VSWH Falling to GL Rising Deadtime	VSWH @ 1V, GL 10%		20		ns
t_{TSSHD}	Tri-State Shutdown Delay	TS to GH Falling, TS to GL Falling		175		ns
t_{PTS}	Tri-State Propagation Delay	TS Exit		35		ns
t_{LGMIN}	Low-Side Minimum On-Time	FCCM = 0V		350		ns

Notes:

4. All voltages are specified with respect to the corresponding PGND pin
5. Characterisation value. Not tested in production.

Timing Diagram

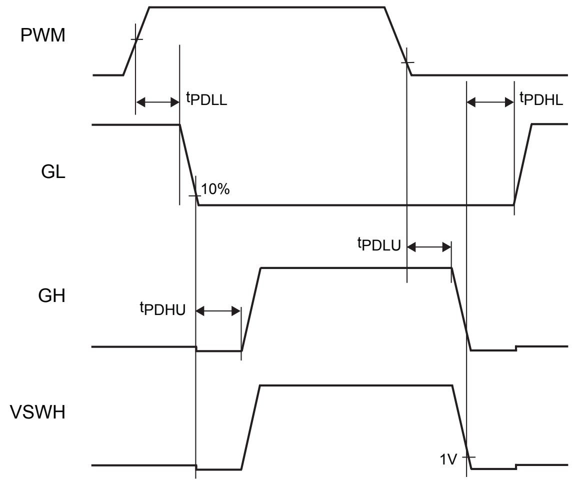


Figure 1. PWM Logic Input Timing Diagram

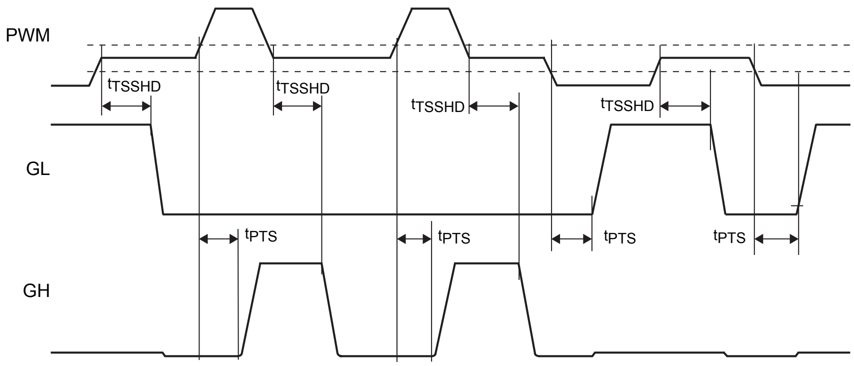


Figure 2. PWM Tri-State Input Logic Timing Diagram

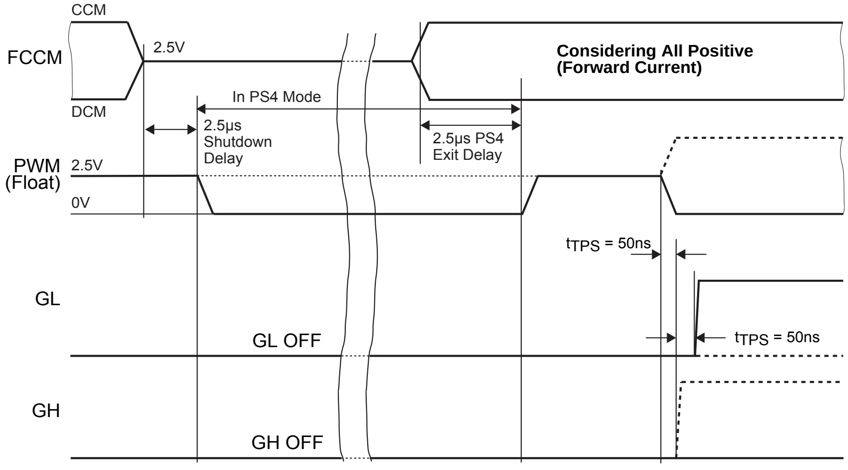


Figure 3. FCCM Logic During High Impedance at PWM Input

Typical Performance Characteristics

T_A = 25°C, V_{IN} = 19V, VCC = 5V, L = 220nH, unless otherwise specified.

Figure 4. 800kHz Efficiency vs. Load Current

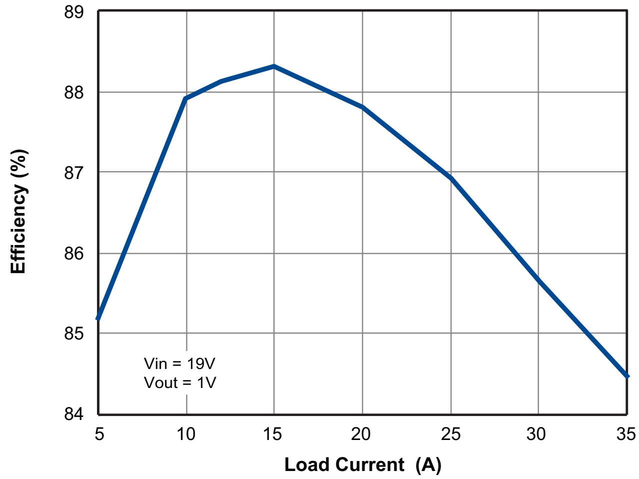


Figure 5. 800kHz Power Loss vs. Load Current

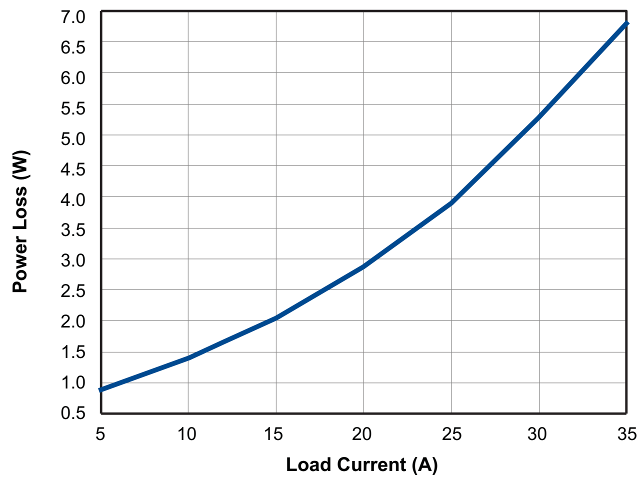


Figure 6. PWM Threshold vs. Temperature

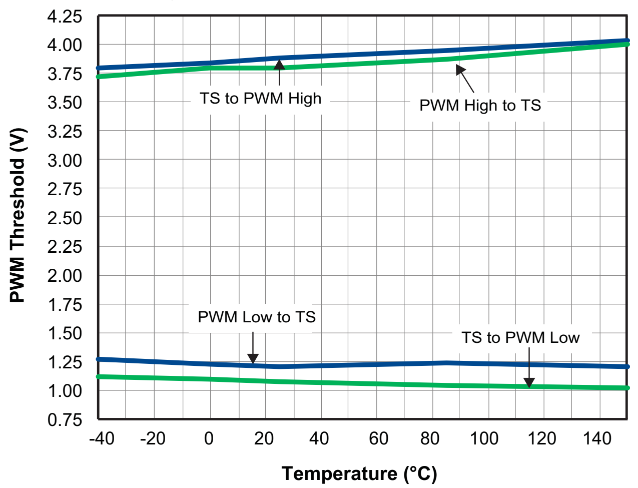


Figure 7. FCCM Input Threshold vs. Temperature

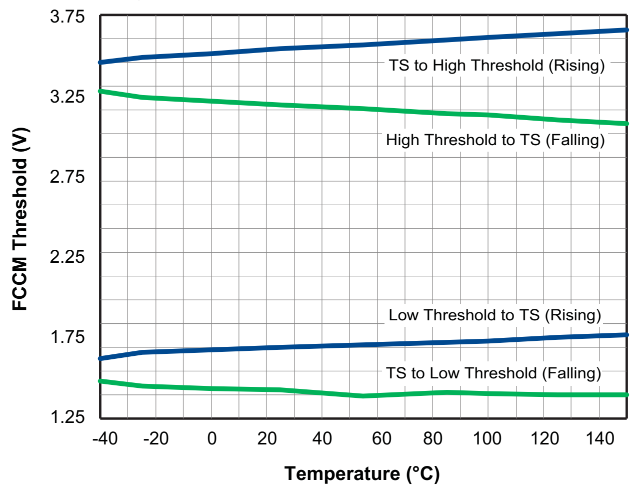


Figure 8. UVLO (V_{CC}) Threshold vs. Temperature

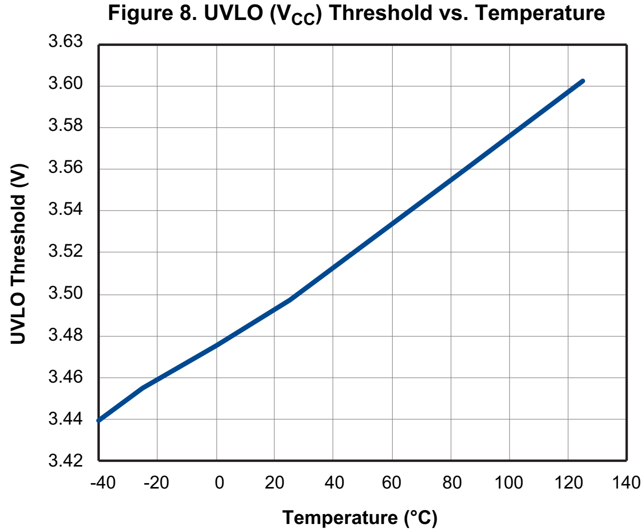
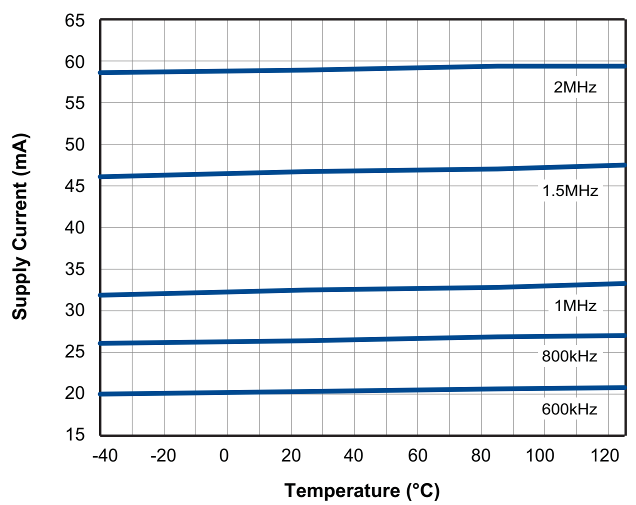
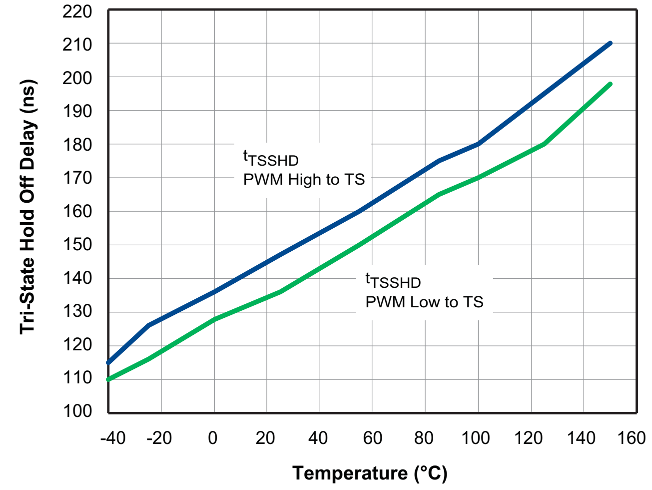


Figure 9. Supply Current (I_{VCC}) vs. Temperature



Typical Performance Characteristics (Continued)

Figure 10. Hold Off Propagation Delay vs. Temperature



Application Information

AOZ5049QI is a fully integrated power module designed to work over an input voltage range of 4.5V to 25V with a separate 5V supply for gate drive and internal control circuits. A number of features make AOZ5049QI a highly versatile power module. The MOSFETs are individually optimized on either HS or LS switches in a low duty cycle synchronous buck converter. A high current driver is also included in the package which minimizes the gate drive loop and results in extremely fast switching. The modules are fully compatible with Intel DrMOS specification IMVP8 in form fit and function.

Powering the Module and the Gate Drives

An external supply VCC of 5V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The integrated gate driver is capable of supplying large peak current into the LS MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 1µF or higher is recommended from VCC to PGND. For effective filtering it is strongly recommended to have a direct connection from this capacitor to PGND (pin 21).

The boost supply for driving the HS MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node VSWH. It is recommended that this capacitor Cboot be connected as close as possible to the device across pins 2 and 5. Boost diode is integrated into the package. A resistor in series with Cboot can be optionally used by designers to slow down the turn on speed of the HS MOSFET. Typically values between 1Ω to 5 Ω is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible.

Undervoltage Lockout

In a UVLO event, both GH and GL outputs are actively held low until adequate gate supply becomes available. The under-voltage lockout is set at 3.4V with a 500mV hysteresis. The AOZ5049QI must be powered up and enabled before the PWM input is applied.

Since the PWM control signals are provided typically from an external controller or a digital processor, extra care must be taken during start up. It should be ensured that PWM signal goes through a proper soft start sequence to minimize inrush current in the converter during start up. Powering the module with a full duty cycle PWM signal may lead to a number of undesirable consequences as explained below. In general it should be noted that AOZ5049QI is a combination of two MOSFETs with an IMVP8 compliant driver, all of which are optimized for switching at the highest efficiency. Other than UVLO and thermal protection, it does not have any monitoring or protection functions built in. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

Input Voltage VIN

AOZ5049QI is rated to operate over a wide input range of 4.5V to 25V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply very closely to package leads with X7R or X5R quality ceramic capacitors.

The HS MOSFET in AOZ5049QI is optimized for fast switching with low duty ratios. It has ultra low gate charges which have been achieved as a trade off with higher $R_{DS(ON)}$ value. When the module is operated at low VIN the duty ratio will be higher and conduction losses in the HS MOSSFET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the HS MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the HS MOSFET may be much hotter than the LS MOSFET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

PWM Input

AOZ5049QI is offered to be interfaced with 5V (TTL) PWM logic. Refer to Figure 1 for the timing and propagation delays between the PWM input and the MOSFET gate drives.

The PWM is also a tri-state compatible input. When the input is high impedance or unconnected both the gate drives will be off and the gates are held active low. The PWM Threshold Table below, lists the thresholds for high and low level transitions as well as tri-state operation window. As shown in Figure 2, there is a hold off delay between the corresponding PWM tri-state signal and the output gate drive being pulled low. This delay is typically 175ns and intended to prevent spurious triggering caused by tri-state mode entrance.

Table 1. PWM Input and Tri-State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5049QI	4.1 V	0.7 V	1.1 V	3.9 V

Note: See Figure 2 for propagation delays and tri-state window.

Diode Mode Emulation of Low Side MOSFET (FCCM)

AOZ5049QI can be operated in the diode emulation or skip mode using the FCCM pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If FCCM is taken high, the controller will use the PWM signal as reference and generate both the high and low side complementary gate drive outputs with the minimal anti-overlap delays necessary to avoid cross conduction. When the pin is taken low the HS MOSFET drive is not affected but diode emulation mode is activated for the LS MOSFET. See Table 2 for all possible logic inputs and corresponding output drive conditions. A high impedance state at the FCCM pin shuts down the AOZ5049QI. The FCCM Threshold Table (Table 3) lists the thresholds for high and low level transitions as well as tri-state threshold window. The FCCM/PWM Timing Diagram in Figure 3 illustrates the sequential timing involved when the PWM pin is left at a high impedance state by the master controller. During a shutdown event (FCCM entering tri-state), the PWM will be actively pulled low by an internal sink circuit of the DrMOS. Nevertheless, the ultimate goal is to ensure that the GH and GL are held at a low state.

Table 2. Control Logic Truth Table

FCCM	PWM	GH	GL
L	L	L	L
L	H	H	L
H	L	L	H
H	H	H	L
L	Tri-State	L	L
H	Tri-State	L	L
Tri-State	X	L	L

Table 3. FCCM Input and Tri-State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5049QI	3.8 V	1.2 V	1.4 V	3.4 V

Note: Diode emulation mode is activated when FCCM pin is held low.

Gate Drives

AOZ5049QI has an internal high current high speed driver that generates the floating gate drive for the HS MOSFET and a complementary drive for the LS MOSFET. Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. An internal shoot through protection scheme ensures that neither MOSFET turns on while the other one is still conducting, thereby preventing shoot through condition of the input current. When the PWM signal makes a transition from H to L or L to H, the corresponding gate drive GH or GL begins to turn off. The adaptive timing circuit monitors the falling edge of the gate voltage and when the level goes below 1V, the complementary gate driver is turned on. The dead time between the two switches is minimized, at the same time preventing cross conduction across the input bus. The adaptive circuit also monitors the switching node VSWH and ensures that transition from one MOSFET to another always takes place without cross conduction, even under transient and abnormal conditions of operation.

The gate pins GH and GL are brought out on pins 4 and 19, respectively. However these connections are not made directly to MOSFET gate pads and their voltage measurement may not reflect the actual gate voltage applied inside the package. The gate connections are primarily for functional tests during manufacturing and no connections should be made to them in the application.

PCB Layout Guidelines

AOZ5049QI is a high current module rated for operation up to 2MHz. This requires extremely fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitics of the package or PCB.

While excellent switching speeds are achieved, correspondingly high levels of dV/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the area of the primary switching current loop, formed by the HS MOSFET, LS MOSFET and the input bypass capacitor CIN. The PCB design is somewhat simplified because of the optimized pin out in AOZ5049QI. The bulk of VIN and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by LS MOSFET, output inductor and output capacitor COUT is the next critical parameter, this requires second layer or "Inner 1" should always be an uninterrupted GND plane with sufficient GND vias placed as close as possible to by-pass capacitors GND pads.

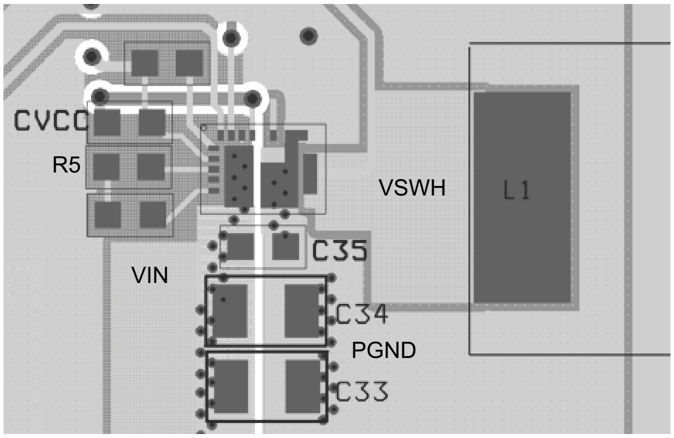


Figure 11. Top Layer of PCB Layout (VIN, VSWH and PGND Copper Planes)

As shown in Figure 11, the top most layer of the PCB should comprise of uninterrupted copper flooding for the primary AC current loop which runs along the VIN copper plane originating from the bypass capacitors C33, C34 and C35 which are mounted to a large PGND copper plane, also on the top most layer of the PCB. These copper planes also serve as heat dissipating elements as heat simply flows down to the VIN exposed pad and onto the top layer VIN copper plane which fans out to a wider area moving away from the 3.5x5 QFN package. Adding vias will only help transfer heat to cooler regions of the PCB board through the other 3 layers (if 4 layer PCB is used) beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

Due to the optimized bonding technique used on the AOZ5049QI internal package, the VIN input capacitors are optimally placed for AC current activities on both the primary and complimentary current loops. The return path of the current during the complimentary period flows through a non interrupted PGND copper plane that is symmetrically proportional to the VIN copper plane.

Due to the PGND exposed pad, heat is optimally dissipated simply by flowing down through the vertically structured lower MOSFET, through the exposed PGND pad and down to the PCB top layer PGND copper plane that also fans outward, moving away from the package.

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spikes appear at the VSWH terminal which are caused by the large internal di/dts produced through the in package parastics. To minimize the effects of this interference, the VSWH terminal at which the main inductor L1 is mounted to, is sized just so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH copper plane on the top layer is voided and the shape of this void is replicated descending down through the rest of the layers as shown on Figure 12 which is the bottom layer of the PCB as an example.

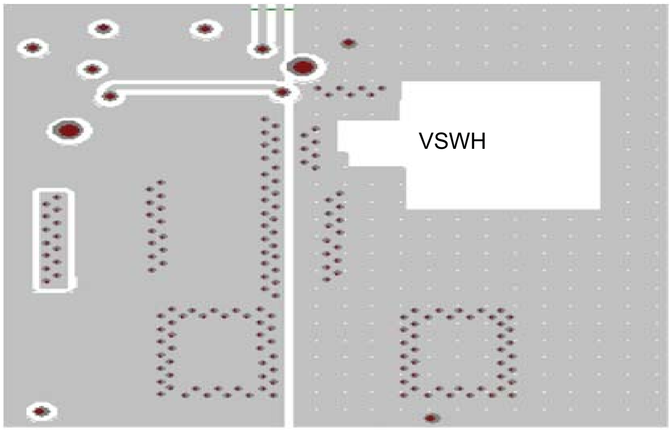


Figure 12. Bottom Layer PCB Layout (VSWH Copper Plane Voided on Descending Layers)

Adding Vias Through Exposed Pads Landing Pattern

The AOZ5049QI can be operated at a switching frequency of up to 2MHz. This implies that the inherent capacitive parameters of the HS and LS MOSFETs need to be charged and discharge on each and every cycle. Due to the back and forth conduction of these AC currents flowing in and out of the input capacitors, the exposed pads (VIN and PGND) would tend to heat up, hence requiring thermal venting. Positioning vias through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer.

The exposed pads dimensional footprint of the 3.5x5 QFN package is shown on Figure 13. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter vias. 10mil via diameter is a commonly used as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127µm) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

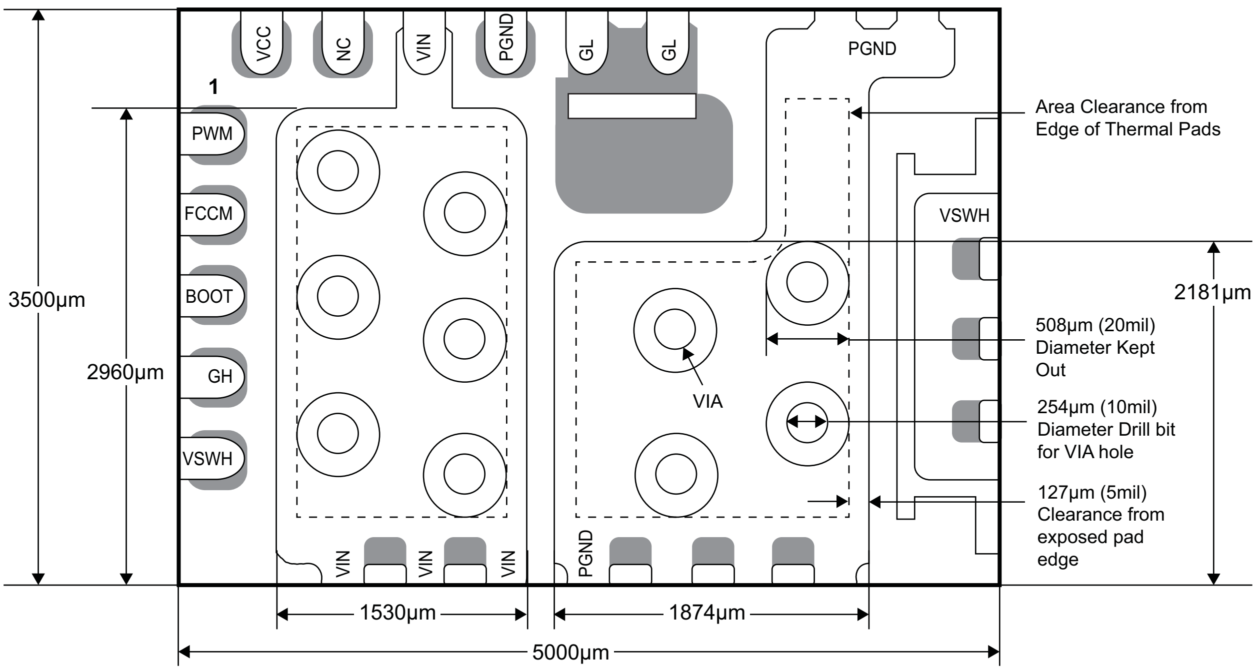
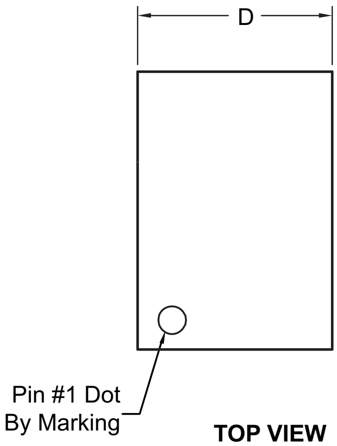
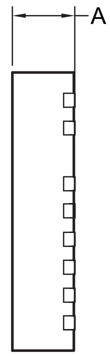


Figure 13. Exposed Pad Land Pattern and Recommended Via Placements

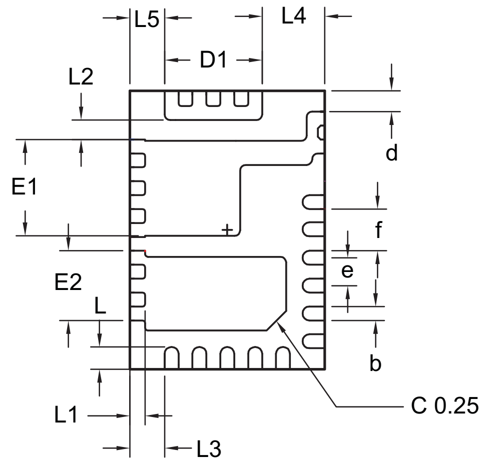
Package Dimensions, QFN3.5x5_24L EP2_S



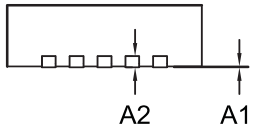
TOP VIEW



SIDE VIEW

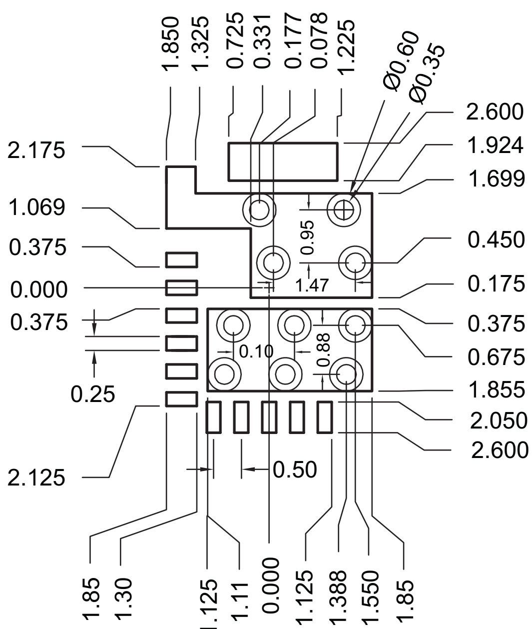


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



Unit: mm

Dimensions in millimeters

Symbols	Min.	Typ.	Max.
A	1.00	1.10	1.20
A1	0.00	-	0.05
A2		0.2 REF	
E	4.90	5.00	5.10
E1	1.63	1.73	1.83
E2	1.15	1.25	1.35
D1	1.65	1.75	1.85
D	3.40	3.50	3.60
L	0.35	0.40	0.45
L1	0.22	0.27	0.32
L2	0.30	0.35	0.40
L3	0.58	0.63	0.68
L4	1.02	1.12	1.22
L5	0.58	0.63	0.68
b	0.20	0.25	0.30
d	0.33	0.38	0.43
f	0.70	0.75	0.80
e		0.50 BSC	

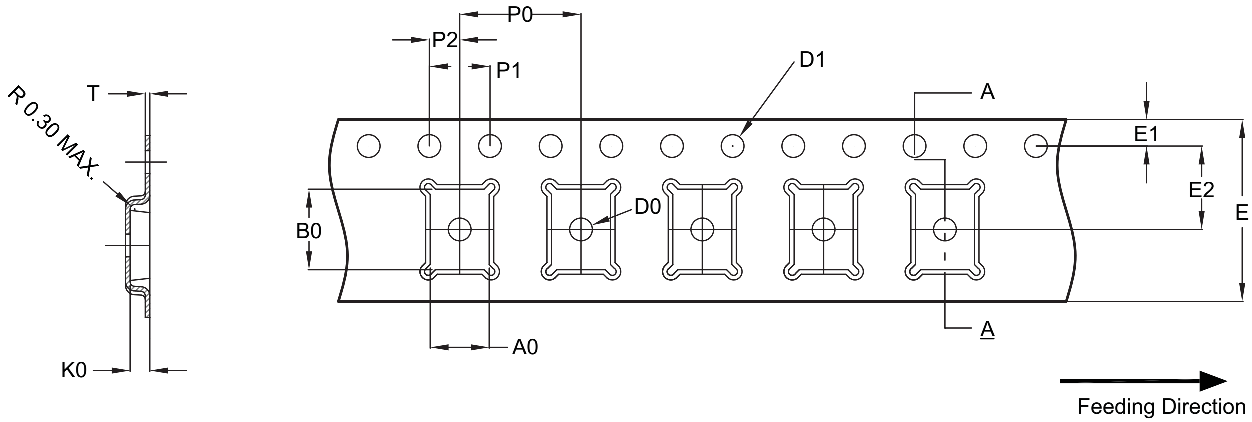
Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.039	0.043	0.047
A1	0.000	-	0.002
A2		0.008 REF	
E	0.193	0.197	0.201
E1	0.064	0.068	0.072
E2	0.045	0.049	0.053
D1	0.065	0.069	0.073
D	0.134	0.138	0.142
L	0.014	0.016	0.018
L1	0.009	0.011	0.013
L2	0.012	0.014	0.016
L3	0.023	0.025	0.027
L4	0.040	0.044	0.048
L5	0.023	0.025	0.027
b	0.008	0.010	0.012
d	0.013	0.015	0.017
f	0.028	0.030	0.031
e		0.02 BSC	

Note:
Controlling dimension are in millimeters. Converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, QFN3.5x5

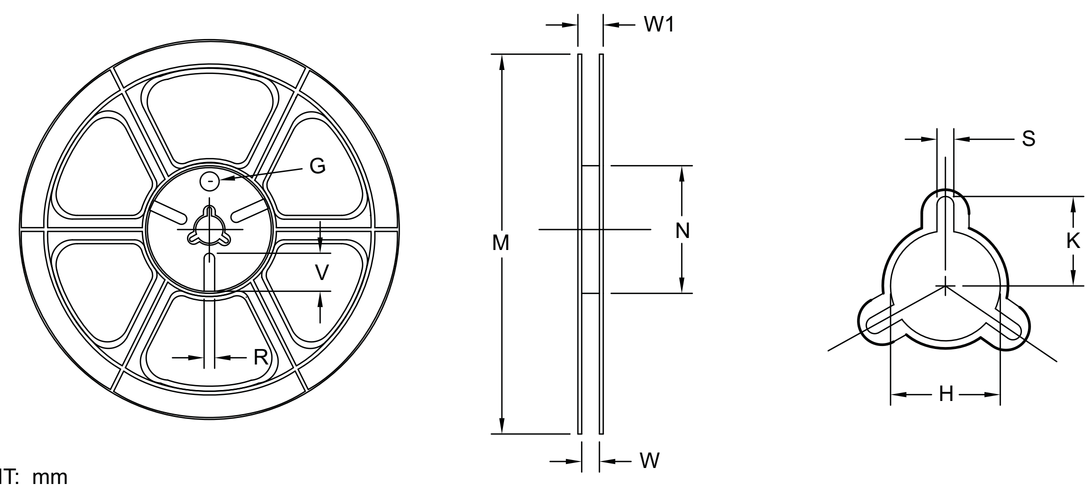
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN3.5x5 (12mm)	3.89 ±0.10	5.31 ±0.10	1.30 ±0.10	1.50 MIN.	1.50 +0.1 -0.0	12.0 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

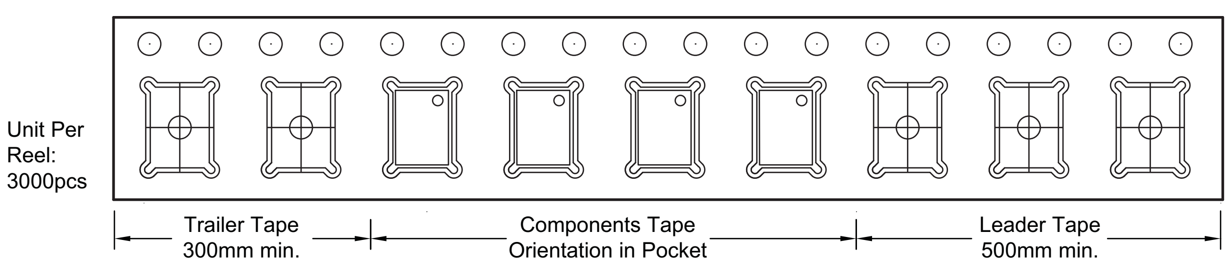
Reel



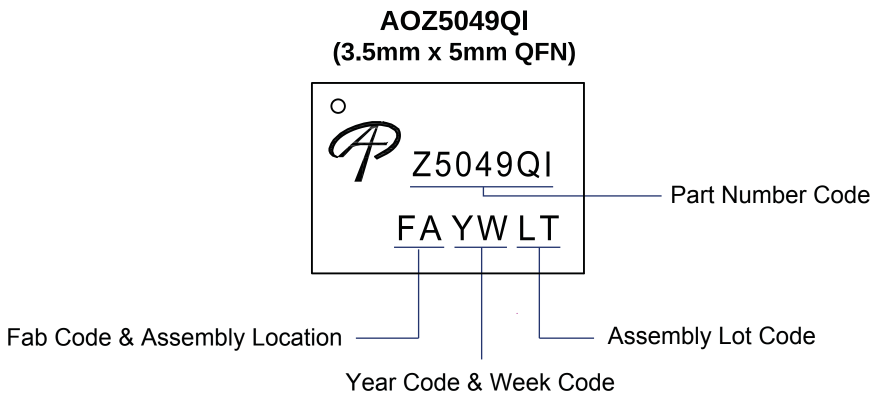
UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	S	K	G	R	V
12mm	Ø330	Ø330 ±2.00	Ø101.6 ±2.00	12.40 +2.00/-0.00	12.40 +3.00/-0.20	Ø13.20 ±0.30	1.70-2.60	---	---	---	---

Leader/Trailer and Orientation



Part Marking



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