PIC32MX534/564/664/764

PIC32MX534/564/664/764 Family
Silicon Errata and Data Sheet Clarification

The PIC32MX534/564/664/764 family devices that you have received conform functionally to the current Device Data Sheet (DS61156**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MX534/564/664/764 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with the REAL ICE™ In-Circuit Emulator:

1. Using the appropriate interface, connect the device to the REAL ICE In-Circuit Emulator.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX534/564/664/764 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A0	A1
PIC32MX534F064H	0x4400053	0x0	0x1
PIC32MX564F064H	0x4401053	0x0	0x1
PIC32MX564F128H	0x4403053	0x0	0x1
PIC32MX664F064H	0x4405053	0x0	0x1
PIC32MX664F128H	0x4407053	0x0	0x1
PIC32MX764F128H	0x440B053	0x0	0x1
PIC32MX534F064L	0x440C053	0x0	0x1
PIC32MX564F064L	0x440D053	0x0	0x1
PIC32MX564F128L	0x440F053	0x0	0x1
PIC32MX664F064L	0x4411053	0x0	0x1
PIC32MX664F128L	0x4413053	0x0	0x1
PIC32MX764F128L	0x4417053	0x0	0x1

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"PIC32MX Flash Programming Specification"* (DS61145) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A0	A1
JTAG	—	1.	On 64-pin devices the TMS pin requires an external pull-up.	X	X
CAN	—	2.	The TXBAT bit status may be incorrect after an abort.	X	X
SPI	Slave Mode	3.	The SPIBUSY status is incorrect after an aborted transfer.	X	X
SPI	Slave Mode	4.	A wake-up interrupt may not be clearable.	X	X
SPI	Frame Mode	5.	Recovery from an underrun requires multiple SPI clock periods.	X	X
SPI	—	6.	Byte writes to the SPISTAT register are not decoded correctly.	X	X
UART	—	7.	The TRMT bit is asserted before the transmission is complete.	X	X
UART	IrDA® with BCLK	8.	TX data is corrupted when BRG values greater than 0x200 are used.	X	X
UART	IrDA	9.	The IrDA minimum bit time is not detected at all baud rates.	X	X
UART	UART Receive Buffer Overrun Error Status	10.	The OERR bit does not get cleared on a module Reset.	X	X
ADC	Conversion Trigger from INT0 Interrupt	11.	The ADC module conversion triggers occur on the rising edge of the INT0 signal even when INT0 is configured to generate an interrupt on the falling edge.	X	X
JTAG	Boundary Scan	12.	Pin 100 on 100-pin packages and pin A1 on 121-pin packages do not respond to boundary scan commands.	X	X
Oscillator	Clock Switch	13.	Clock switch may not work if Cache is disabled and Prefetch is enabled.	X	X
DMA	Suspend Status	14.	The DMABUSY status bit may not reflect the correct status if the DMA module is suspended.	X	X
Voltage Regulator	BOR	15.	Device may not exit BOR state if BOR event occurs.	X	X
USB	OTG Mode	16.	When the USB model is configured for OTG operation, it may not properly recognize all required OTG voltage levels on VBUS pin.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: JTAG

On 64-pin devices an external pull-up resistor is required on the TMS pin for proper JTAG.

Work around

Connect a 100k-200k pull-up to the TMS pin.

Affected Silicon Revisions

A0	A1						
X	X						

2. Module: CAN

When an abort request occurs concurrently with a successful message transmission, and additional messages remain in the FIFO, these remaining messages are not transmitted and the TXBAT bit does not reflect the abort.

Work around

The actual FIFO status can be determined by the FIFO pointers CFIFOCI and CFIFOUA.

Affected Silicon Revisions

A0	A1						
X	X						

3. Module: SPI

In Slave mode with Chip Select (CS) enabled, if the Master deasserts CS before the SPI clock has returned to the Idle state, the SPIBUSY bit will remain set until the next SPI data transfer is completed. The other SPI status bits will reflect the actual status.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

4. Module: SPI

In Slave mode when entering Sleep mode after a SPI transfer with SPI interrupts enabled, a false interrupt may be generated waking the device. This interrupt can be cleared; however, entering Sleep may cause the condition to occur again.

Work around

Do not use SPI in Slave mode as a wake-up source from Sleep.

Affected Silicon Revisions

A0	A1						
X	X						

5. Module: SPI

In Frame mode the module is not immediately ready for further transfers after clearing the SPITUR bit. The SPITUR bit will be cleared by hardware before the SPI state machine is prepared for the next operation.

Work around

Firmware must wait at least four bit times before writing to the SPI registers after clearing the SPITUR bit.

Affected Silicon Revisions

A0	A1						
X	X						

6. Module: SPI

Byte writes to the SPISTAT register are not decoded correctly. A byte write to byte zero of SPISTAT is actually performed on both byte zero and byte one. A byte write to byte one of SPISTAT is ignored.

Work around

Only perform word operations on the SPISTAT register.

Affected Silicon Revisions

A0	A1						
X	X						

7. Module: UART

The TRMT bit is asserted during the STOP bit generation not after the STOP bit has been sent.

Work around

If firmware needs to be aware when the transmission is complete, firmware should add a half bit time delay after the TRMT bit is asserted.

Affected Silicon Revisions

A0	A1						
X	X						

8. Module: UART

In IrDA mode with baud clock output enabled, the UART TX data is corrupted when the BRG value is greater than 0x200.

Work around

Use the Peripheral Bus (PB) divisor to lower the PB frequency such that the required UART BRG value is less than 0x201.

Affected Silicon Revisions

A0	A1						
X	X						

9. Module: UART

The UART module is not fully IrDA compliant. The module does not detect the 1.6 µs minimum bit width at all baud rates as defined in the IrDA specification. The module does detect the 3/16 bit width at all baud rates.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

10. Module: UART

The OERR bit does not get cleared on a module reset. If the OERR bit is set and the module is disabled, the OERR bit retains its status even after the UART module is reinitialized.

Work around

The user software must check this bit in the UART module initialization routine and clear it if it is set.

Affected Silicon Revisions

A0	A1						
X	X						

11. Module: ADC

When the ADC module is configured to start conversion on an external interrupt (SSRC<2:0> = 001), the start of conversion always occurs on a rising edge detected at the INT0 pin, even when the INT0 pin has been configured to generate an interrupt on a falling edge (INT0EP = 0).

Work around

Generate ADC conversion triggers on the rising edge of the INT0 signal.

Alternatively, use external circuitry to invert the signal appearing at the INT0 pin, so that a falling edge of the input signal is detected as a rising edge by the INT0 pin.

Affected Silicon Revisions

A0	A1						
X	X						

12. Module: JTAG

Pin 100 on 100-pin packages and pin A1 on 121-pin packages do not respond to boundary scan commands.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

13. Module: Oscillator

Clock switch may not work if Cache is disabled (DCSZ<1:0> = 00 in the CHECON register) and Prefetch is enabled (PREFEN<1:0> not equal '00' in the CHECON register).

Work around

Set wait states to a value of 7 (PFMWS<2:0> = 111 in the CHECON register), perform a clock switch, and then set wait states to the desired value.

Affected Silicon Revisions

A0	A1						
X	X						

14. Module: DMA

If the DMA module is suspended by setting the DMA Suspend bit (SUSPEND) in the DMA Controller Control register (DMACON), the DMA Module Busy Bit (DMABUSY) in the DMACON register may continue to show a Busy status, when the DMA module completes transaction.

Work around

Use the Channel Busy bit (CHBUSY) in the DMA Channel Control Register (DCHxCON) to check the status of the DMA channel.

Affected Silicon Revisions

A0	A1						
X	X						

15. Module: Voltage Regulator

Device may not exit BOR state if BOR event occurs.

Work arounds

Work around 1:

VDD must remain within published specification (see Parameter DC10 of the device data sheet).

Work around 2:

Reset device by providing POR condition.

Affected Silicon Revisions

A0	A1						
X	X						

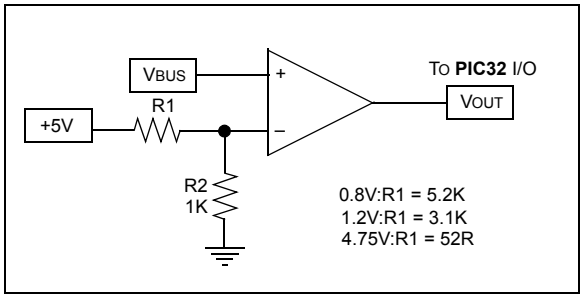
16. Module: USB

When the USB model is configured for OTG operation, it may not properly recognize all required OTG voltage levels on VBUS pin.

Work around

Use external comparator circuit to detect OTG specific voltage levels on VBUS pin.

FIGURE 1: EXTERNAL COMPARATOR SCHEMATIC EXAMPLE



Affected Silicon Revisions

A0	A1						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS61156**G**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None to report at this time.

APPENDIX A: REVISION HISTORY

Rev A Document (7/2010)

Initial release of this document; issued for revision A0 silicon.

Includes silicon issues 1 (JTAG), 2 (CAN), 3-6 (SPI) and 7-9 (UART).

Rev B Document (12/2010)

Added silicon issues 10 (UART), 11 (ADC), 12 (JTAG), 13 (Oscillator), 14 (DMA), 15 (Voltage Regulator) and 16 (USB).

Rev C Document (3/2011)

Updated the data sheet revision from “E” to “F” and updated the current silicon revision to A1 throughout the document.

Added data sheet clarification 1 (Pin Diagrams).

Rev D Document (6/2011)

Updated the data sheet revision from “F” to “G” throughout the document.

Removed data sheet clarification 1.

NOTES:

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